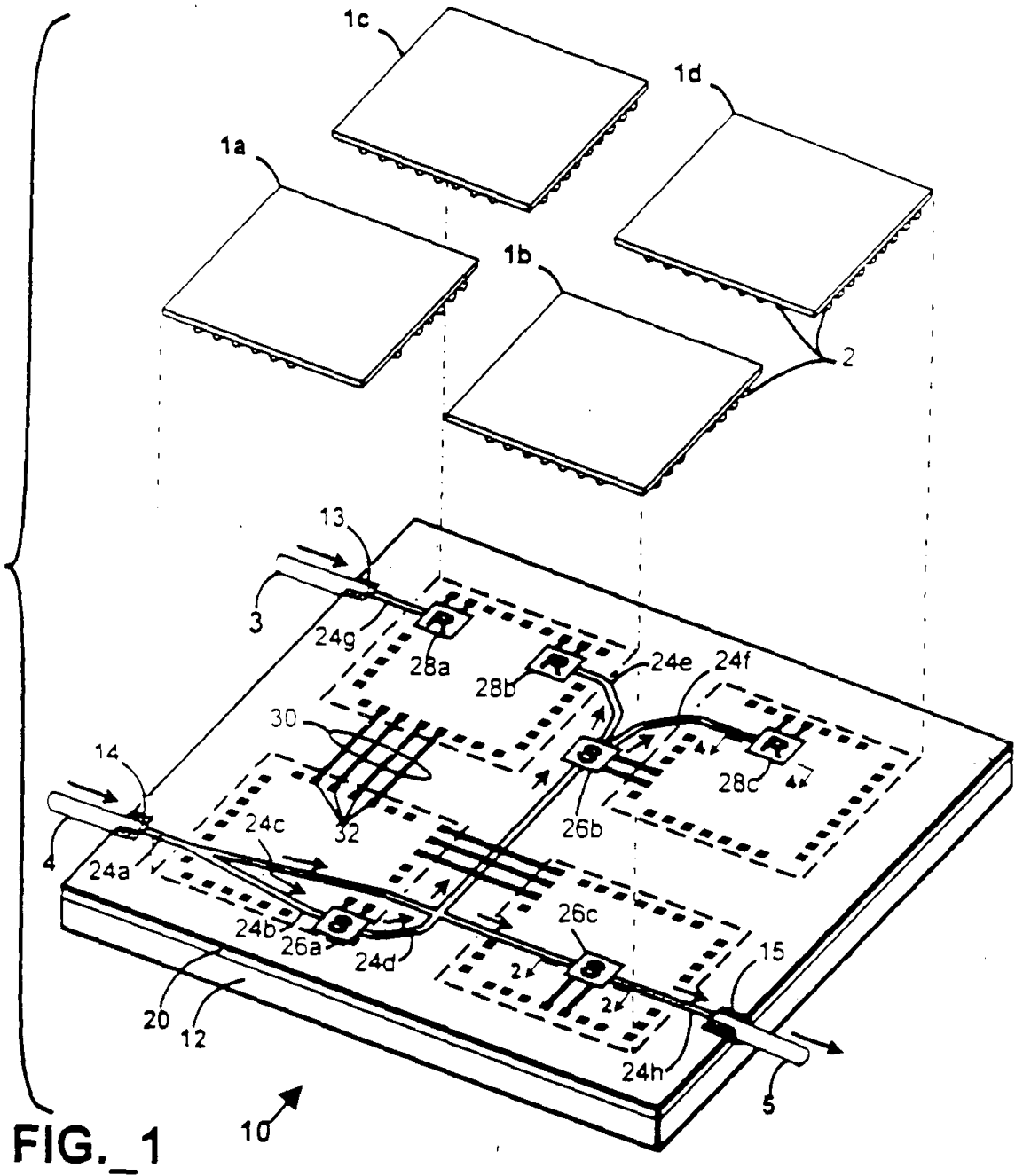


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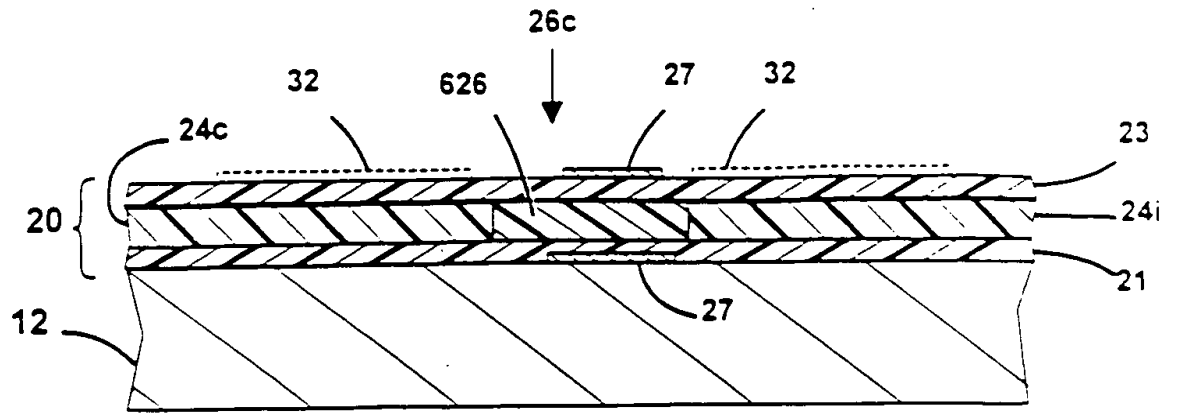


FIG._2

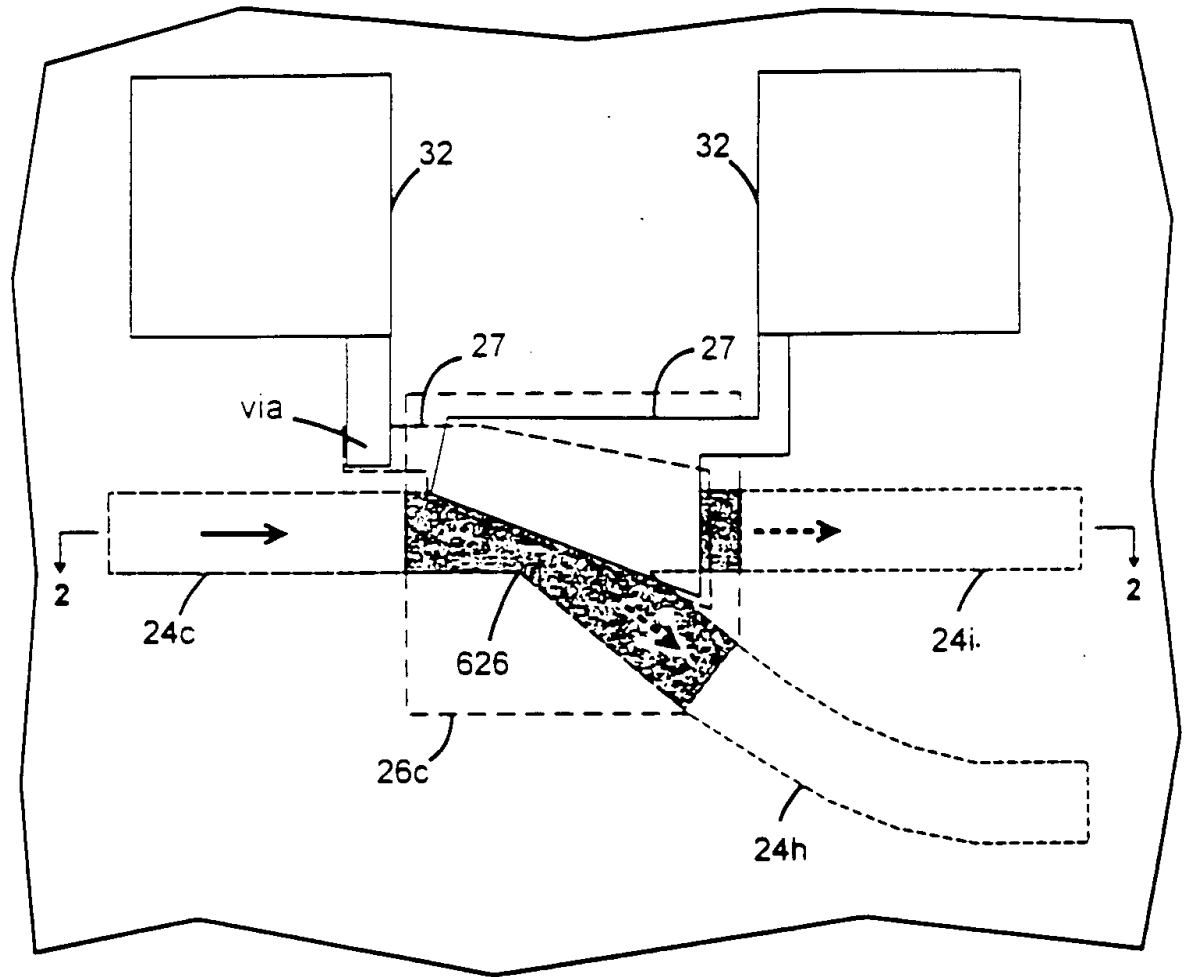


FIG._3

28c'

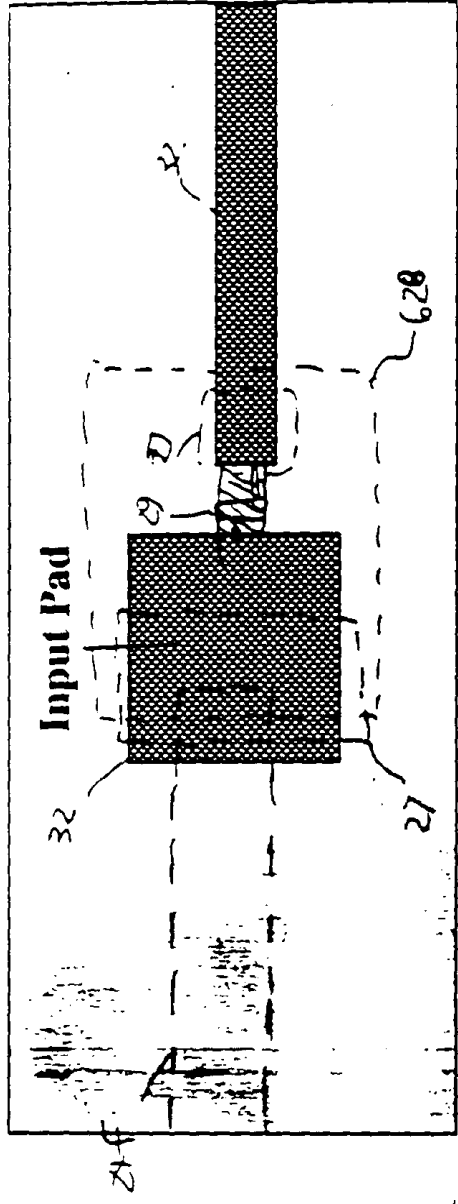


Fig. 5-2

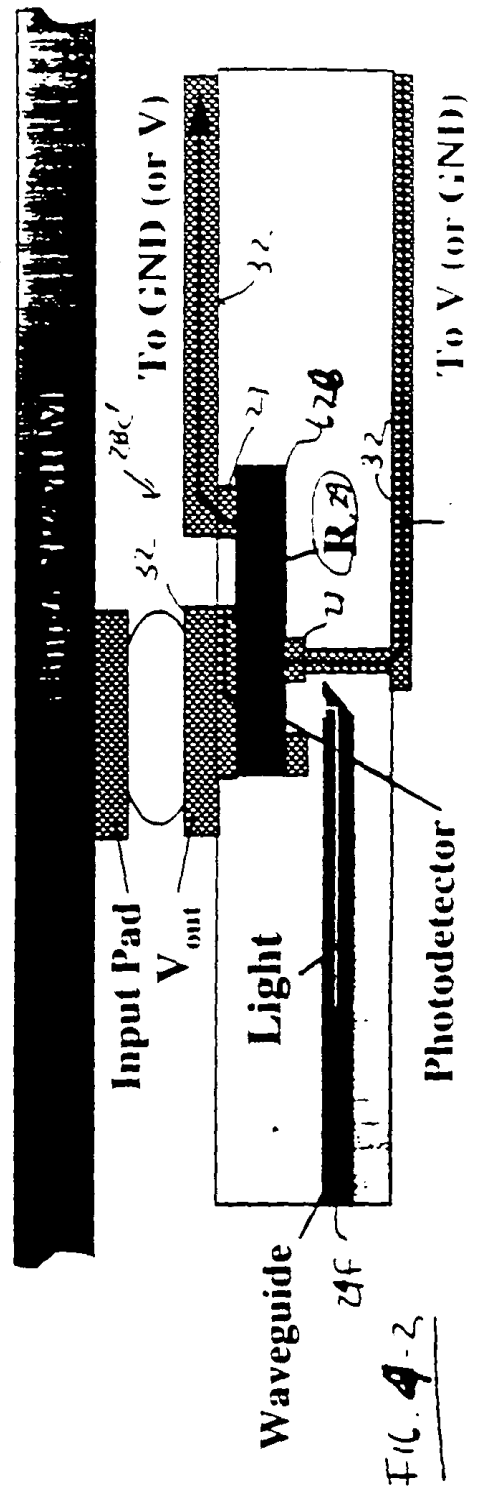


Fig. 4-2

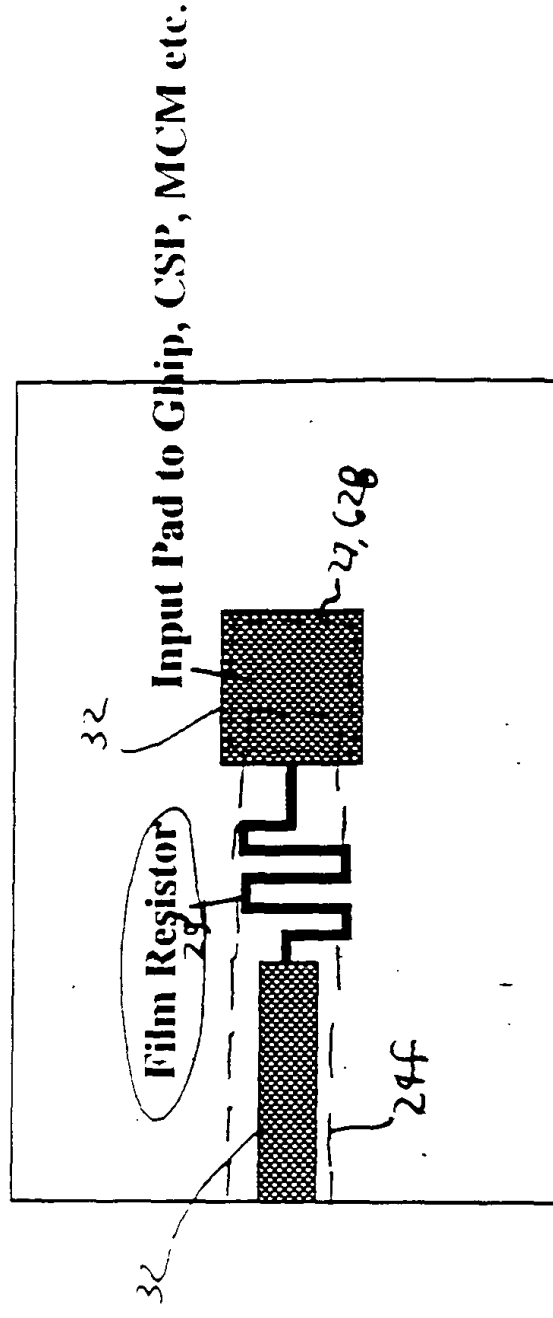


FIG. 5-3

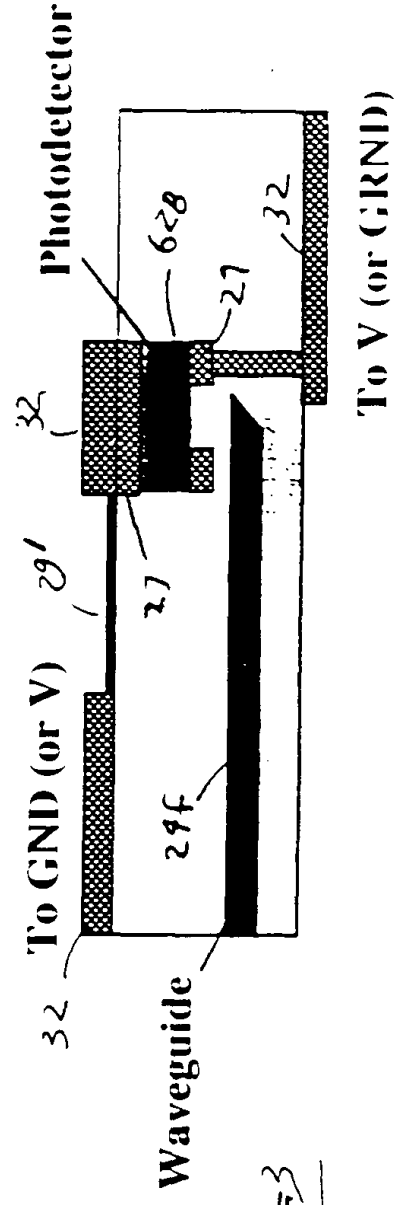


FIG. 4-3

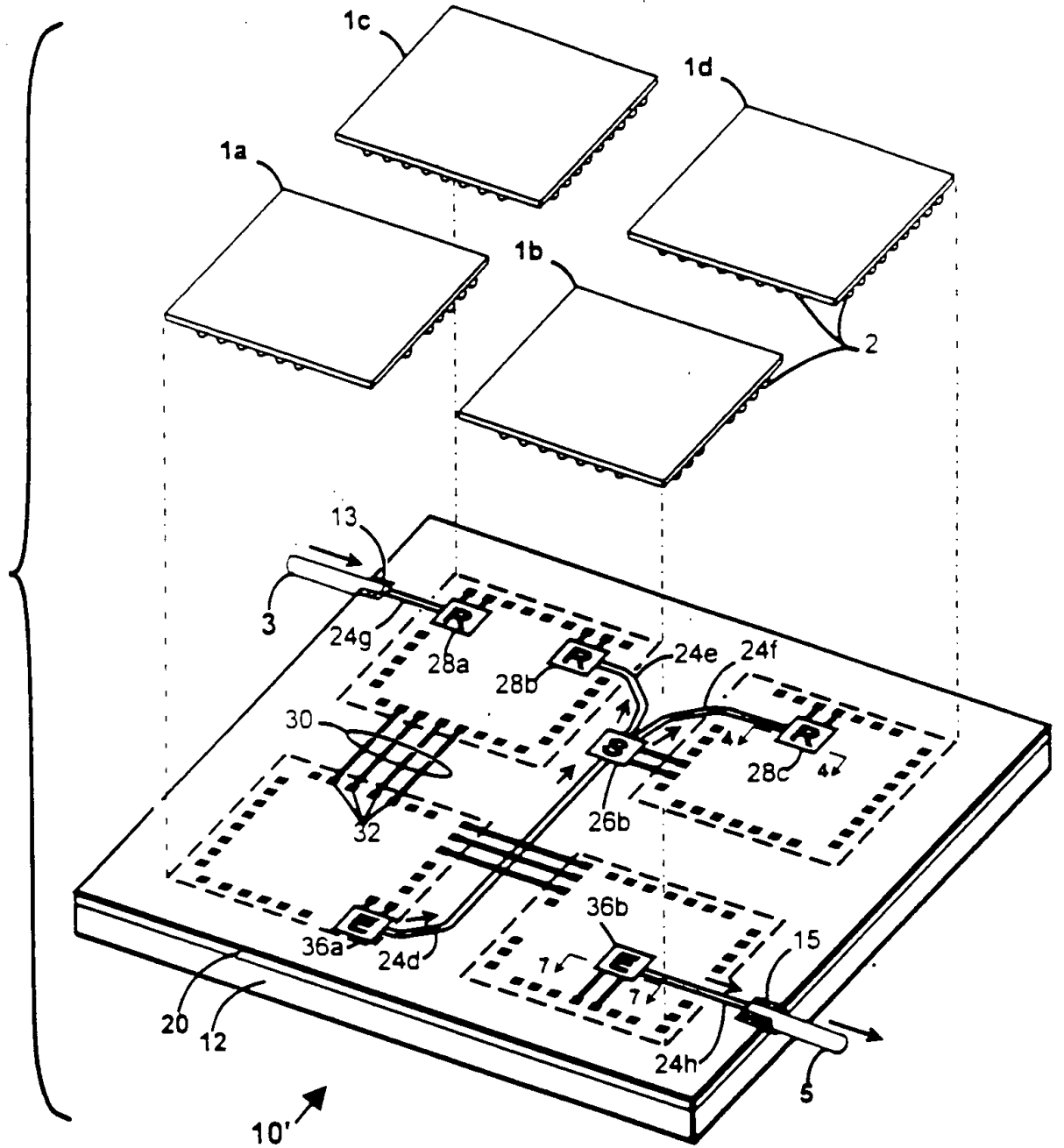


FIG. 6

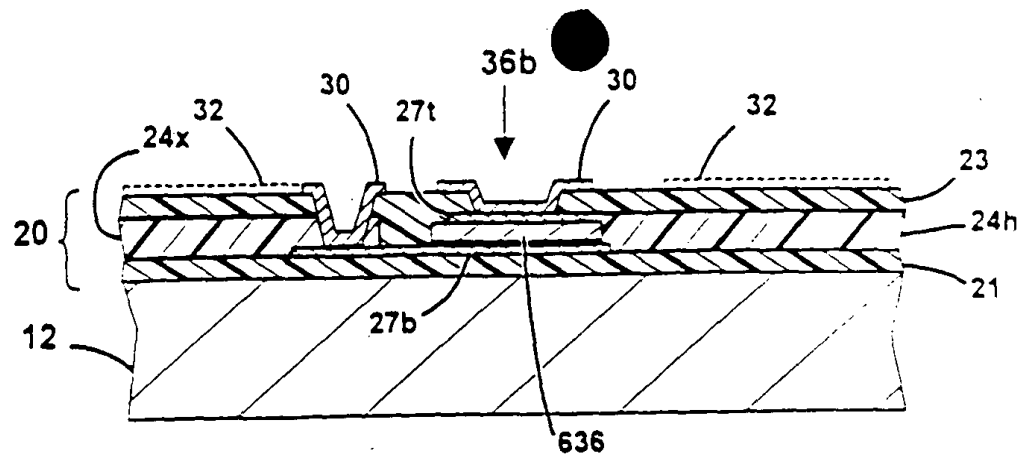


FIG. 7

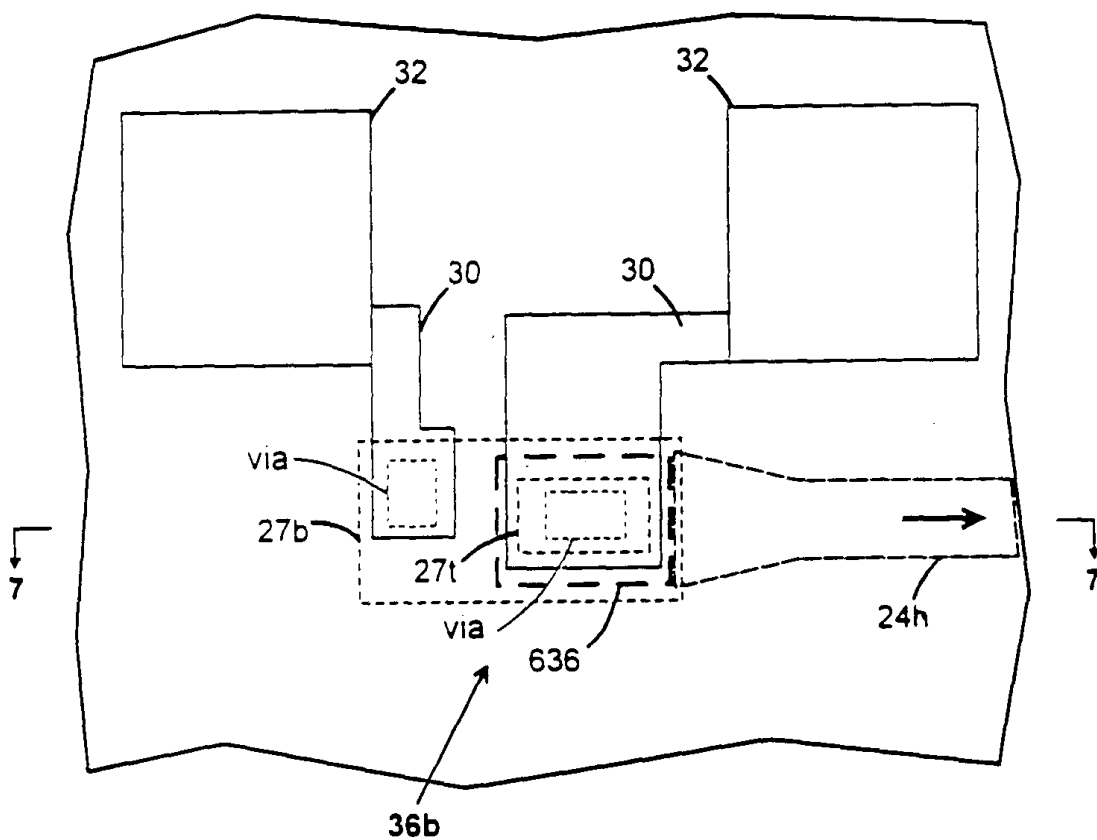
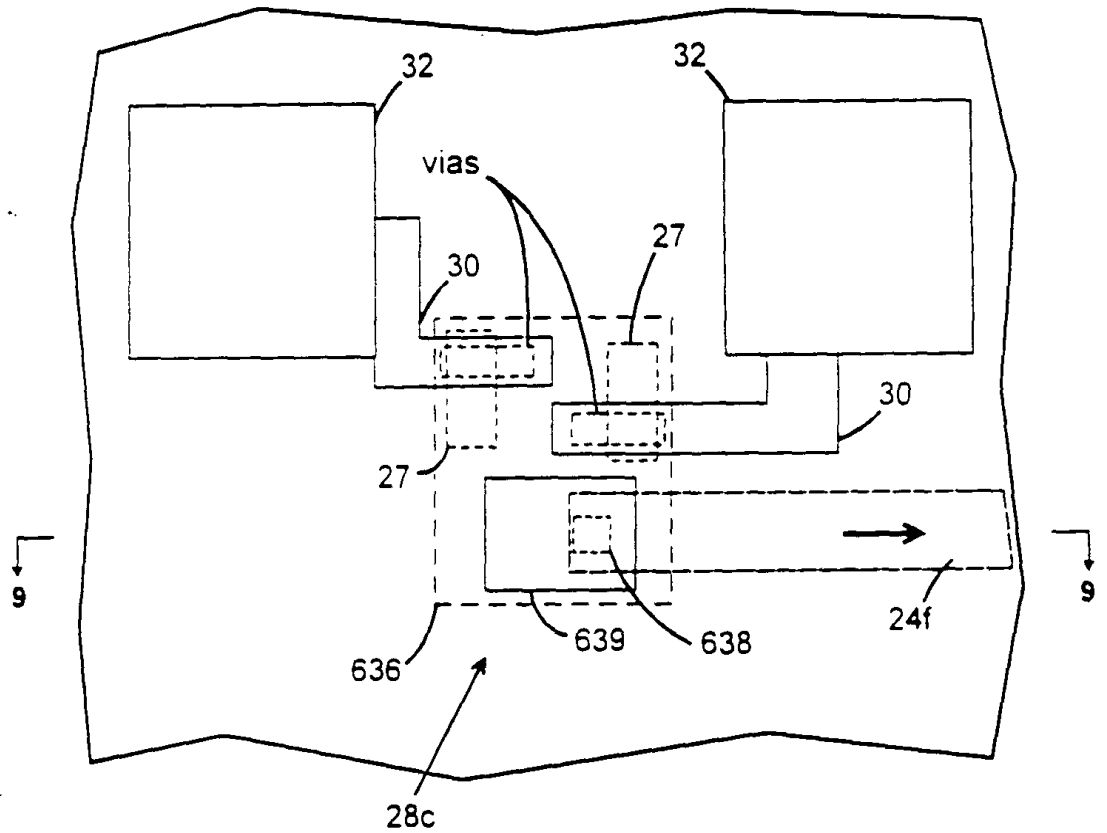
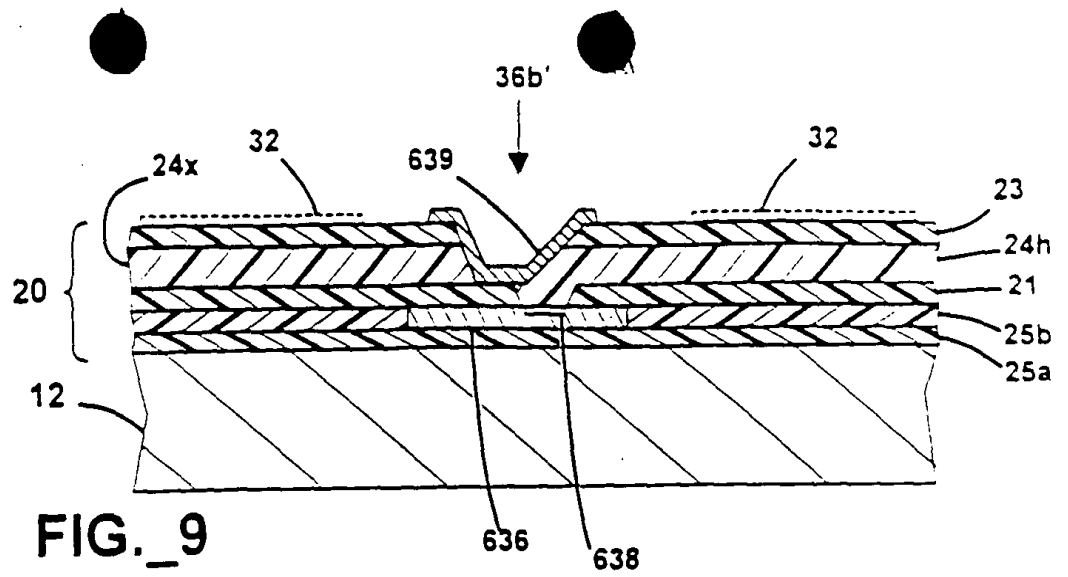


FIG. 8



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FIG. 10-28529260

FIG._11

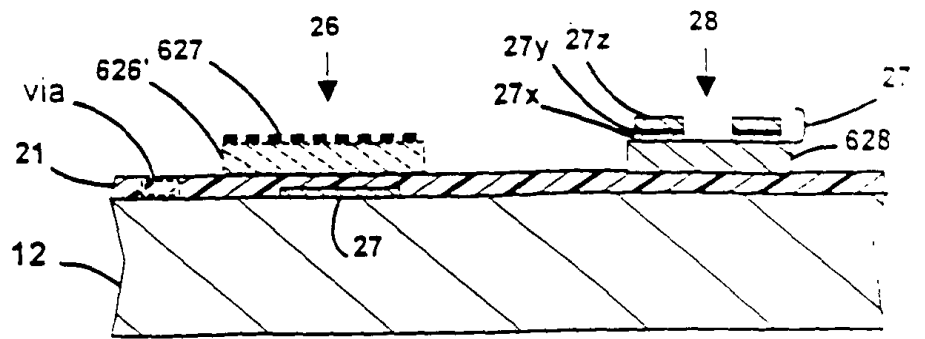


FIG._12

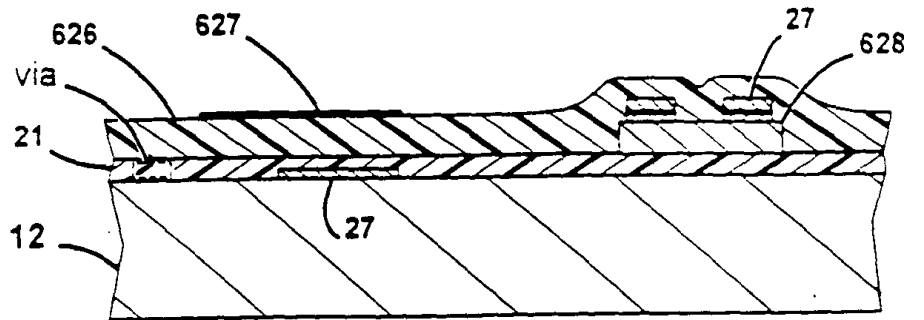


FIG._13

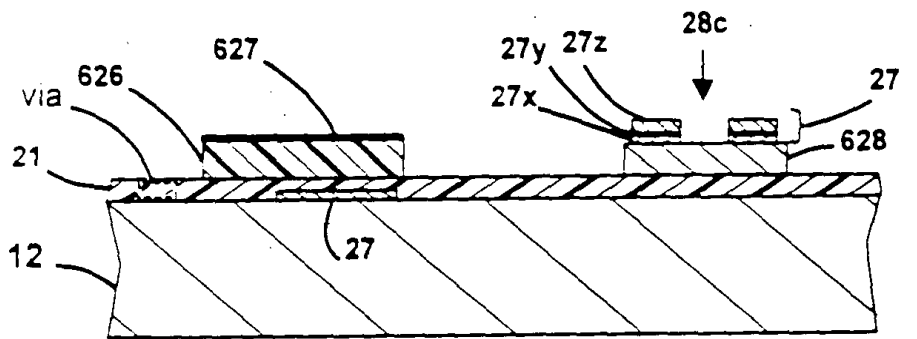
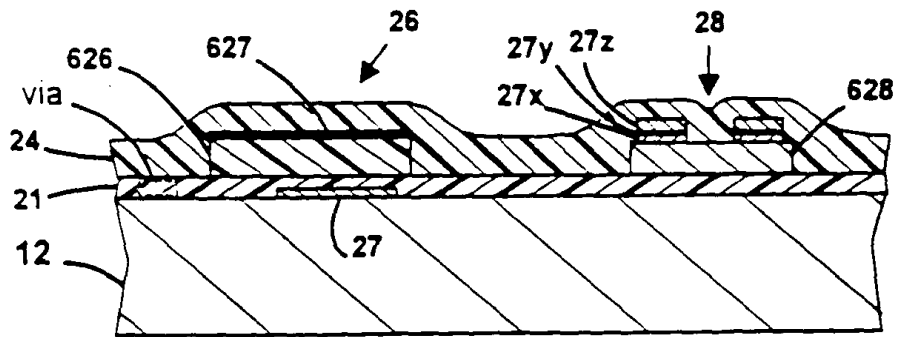


FIG._14



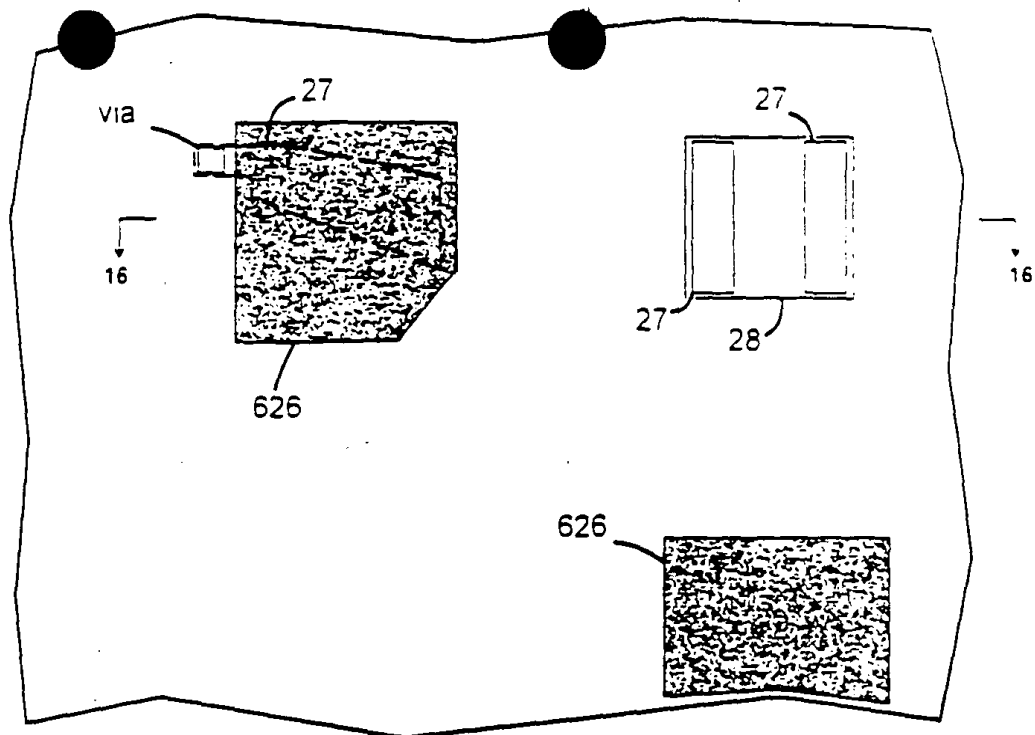


FIG. 19

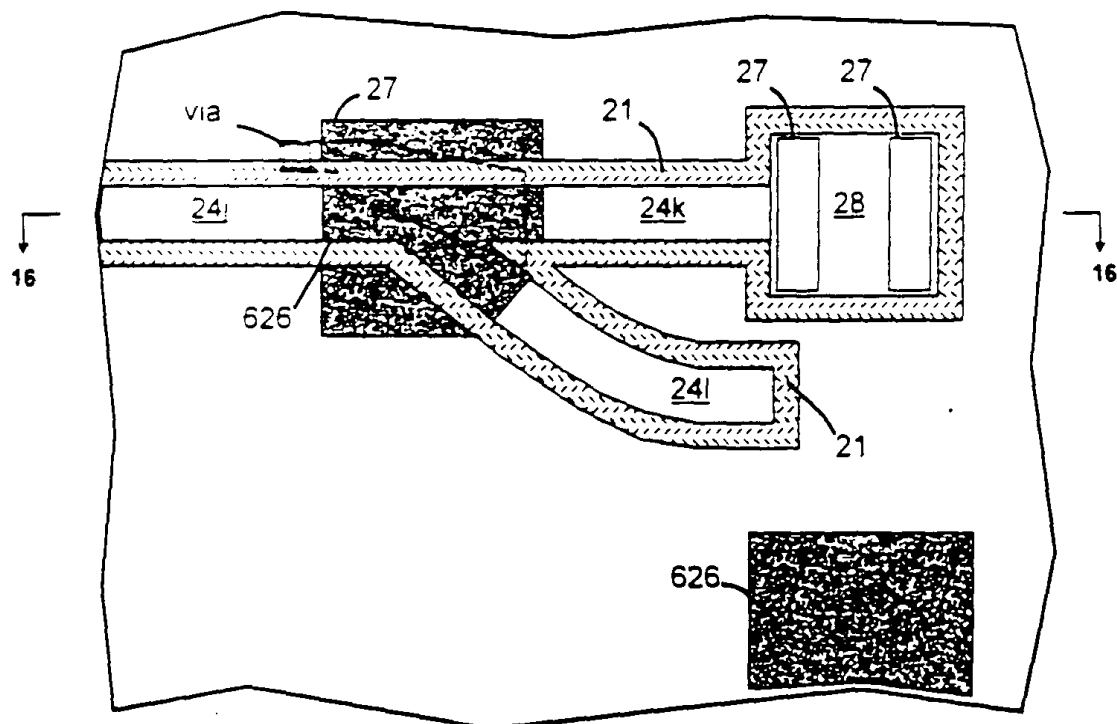


FIG. 20

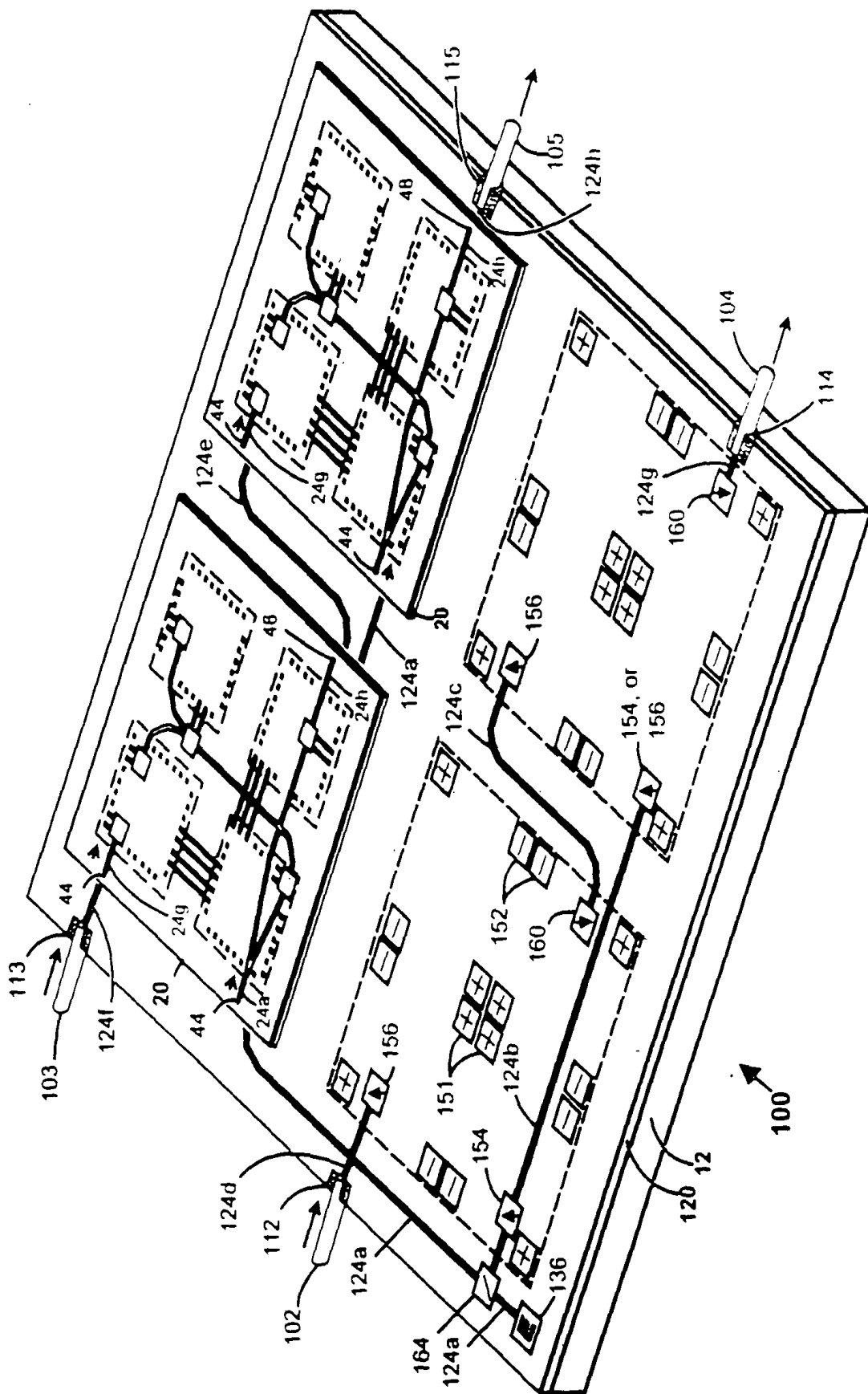


FIG. 21

[illegible]

FIG. 23

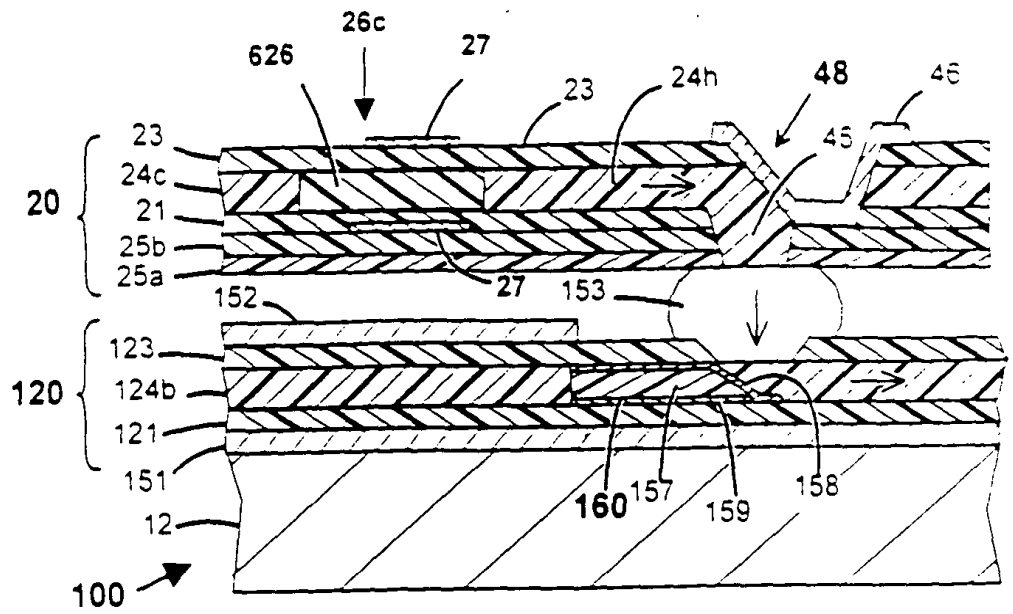


FIG. 24

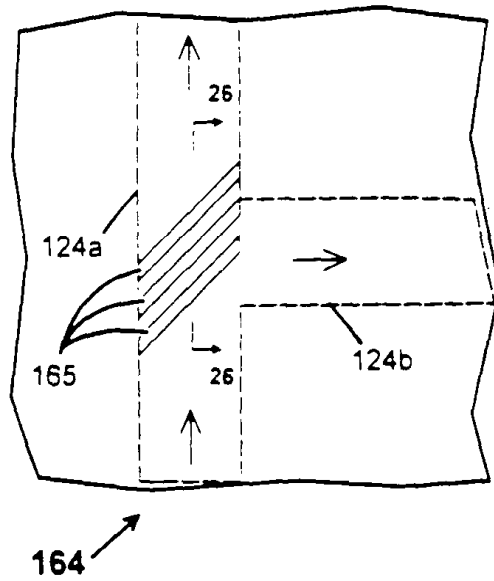


FIG. 25

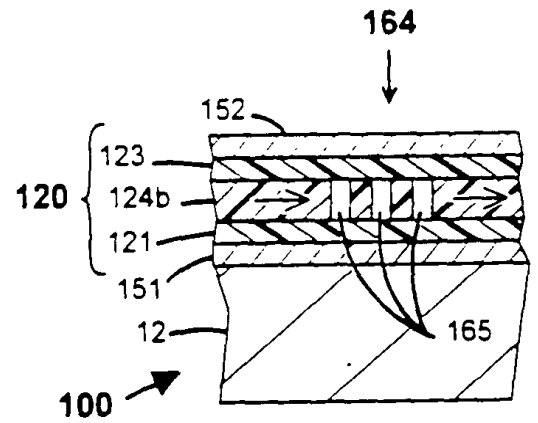


FIG. 26

FIG._27

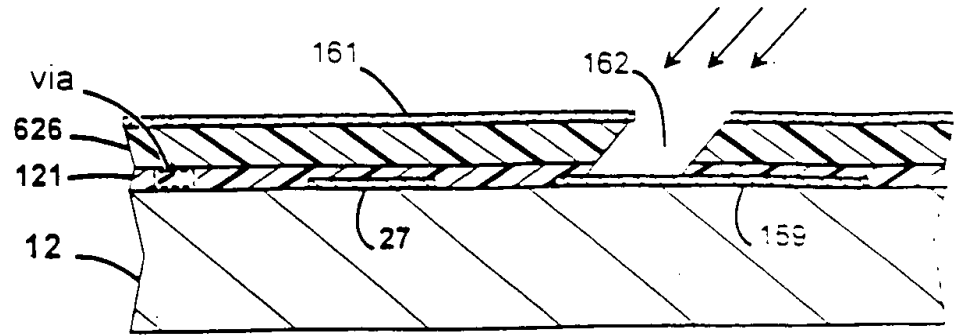


FIG._28

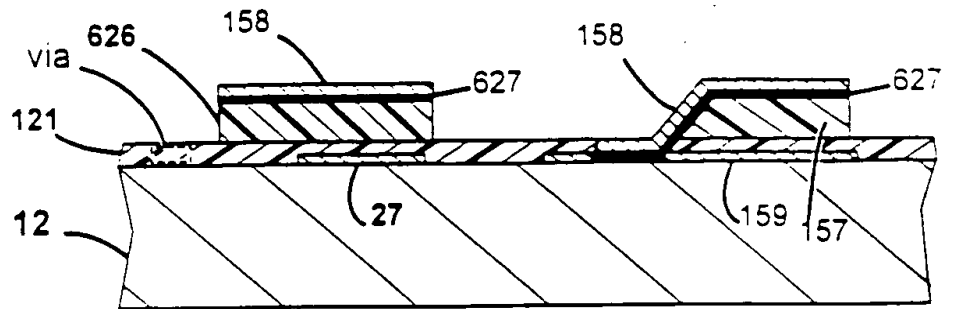


FIG._29

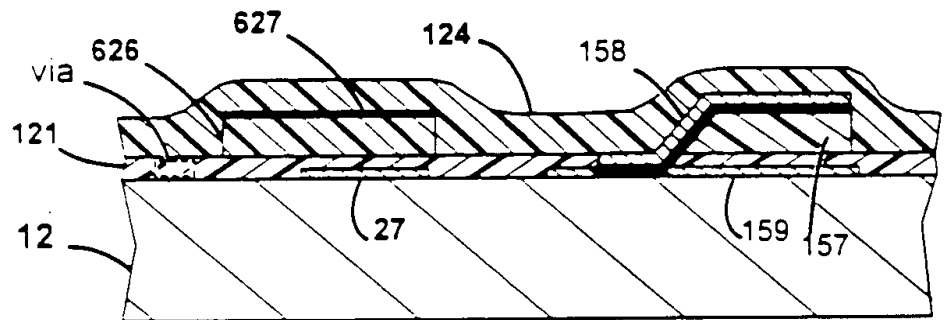
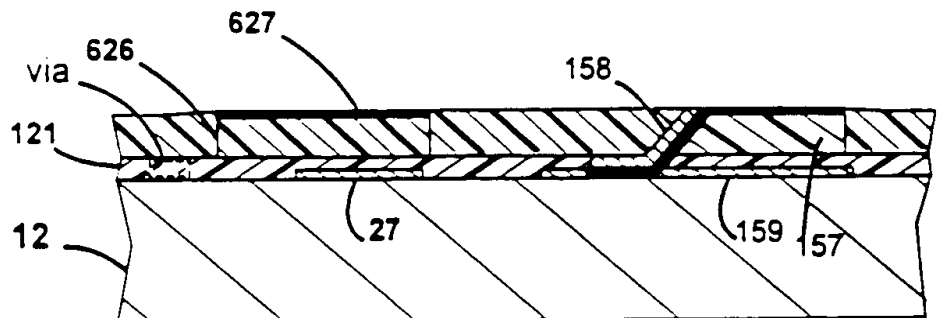


FIG._30



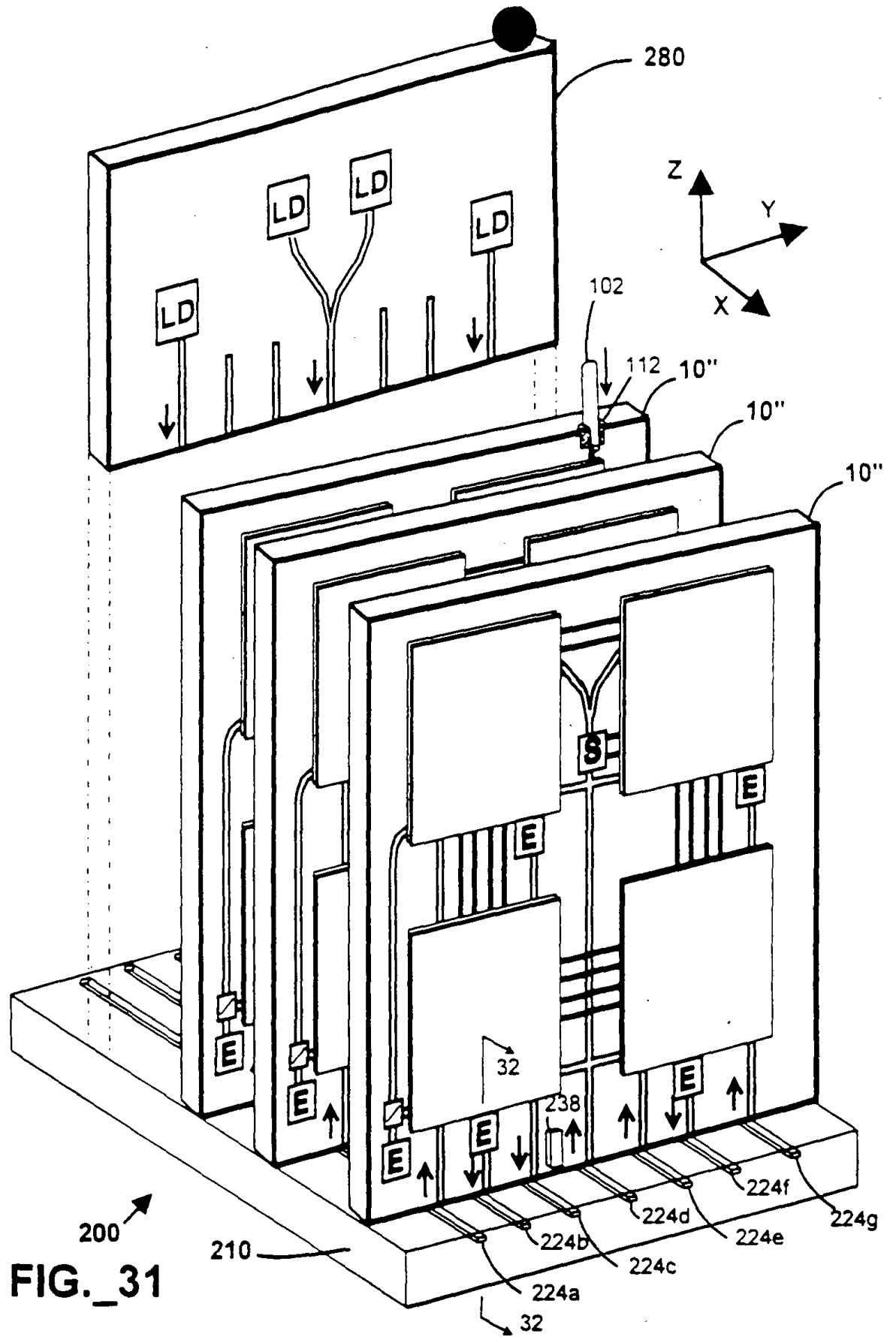
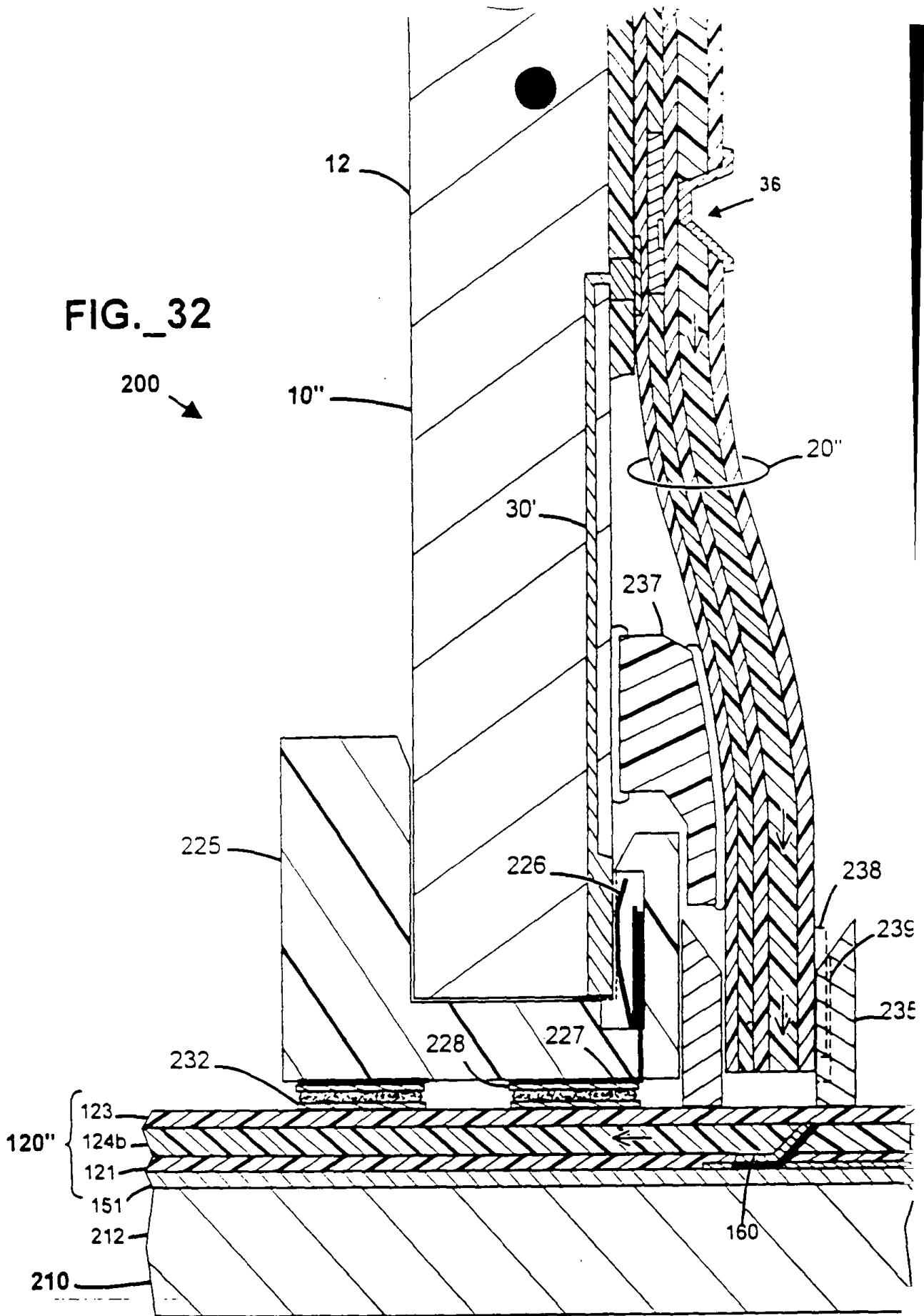


FIG. 31

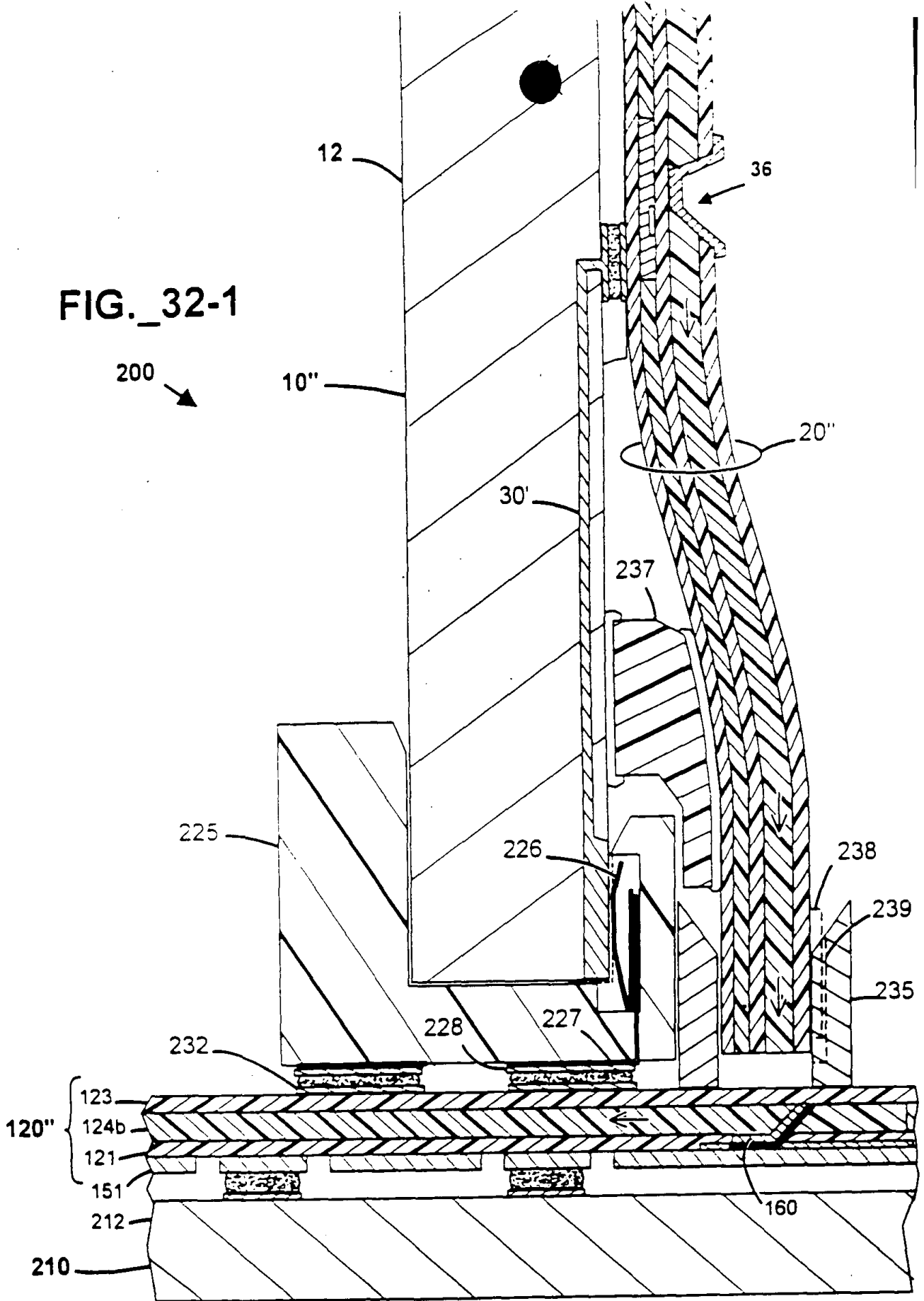
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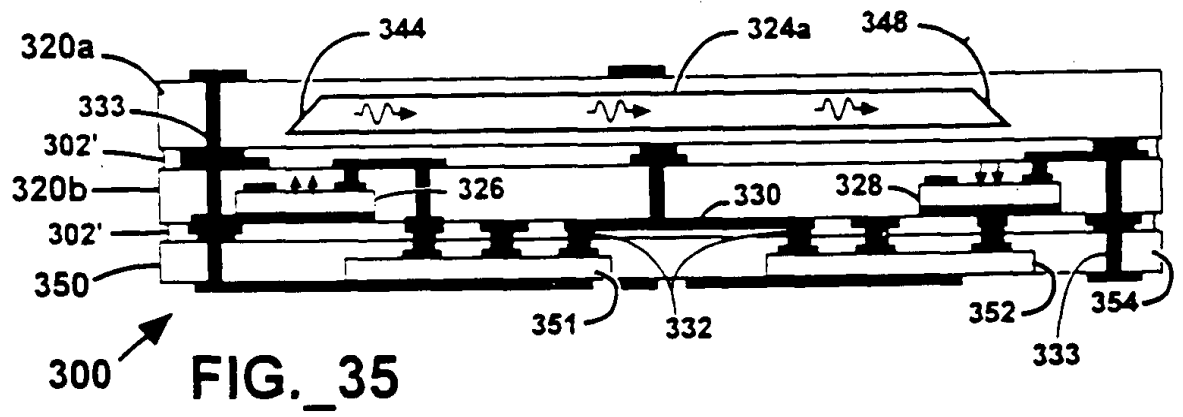
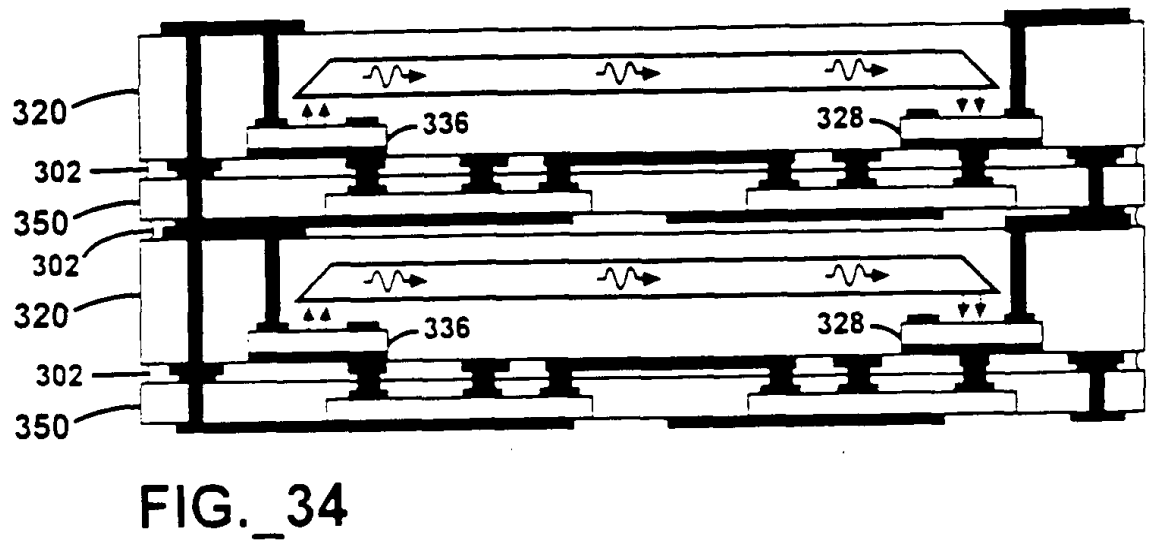
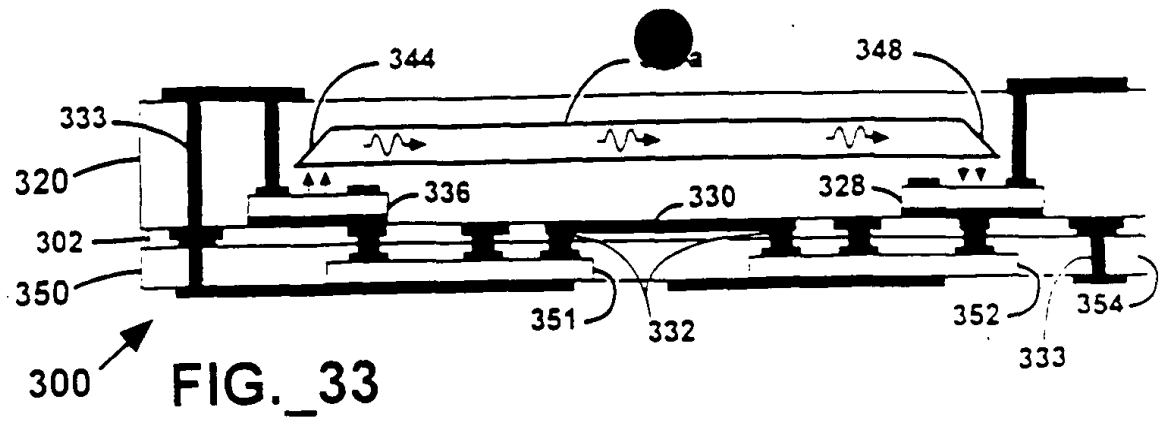
FIG._32



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FIG._32-1





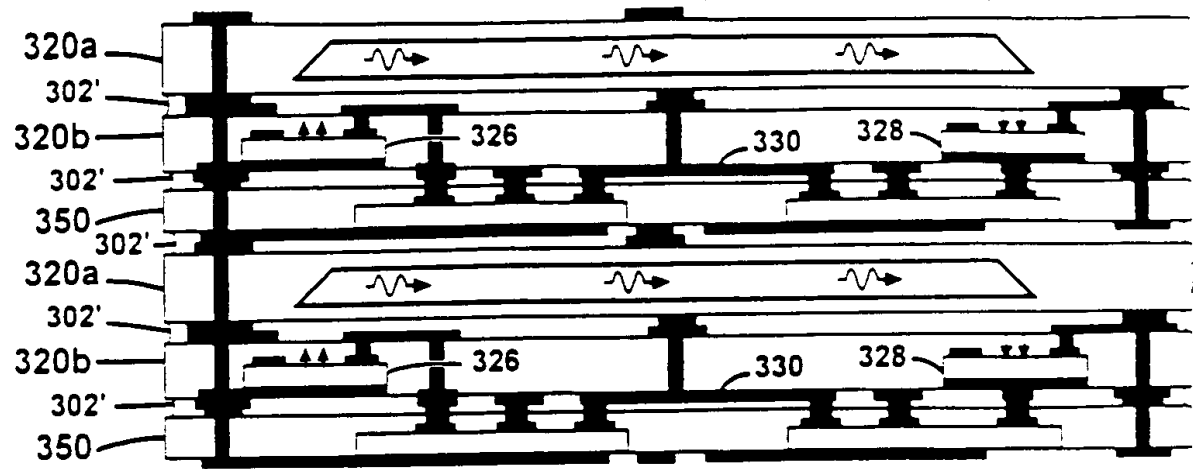


FIG. 36

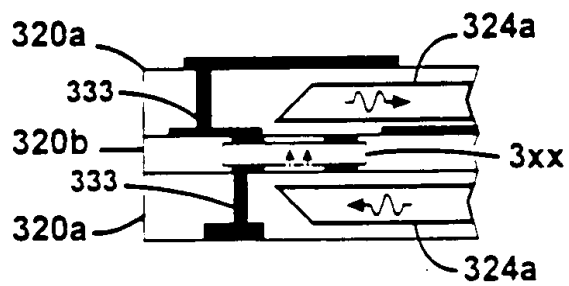


FIG. 37-1

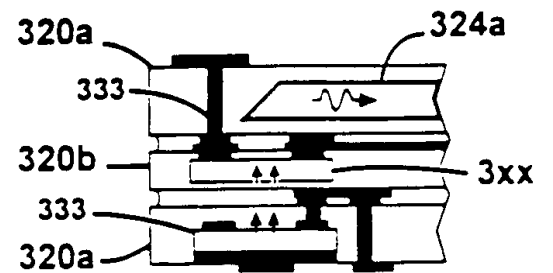


FIG. 37-2

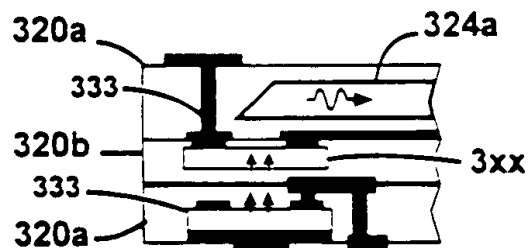


FIG. 37-3

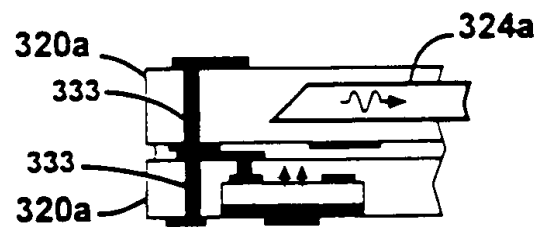


FIG. 37-4

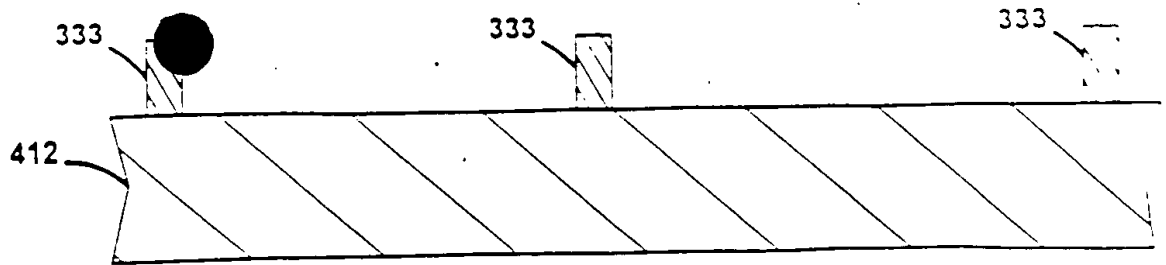


FIG. 38

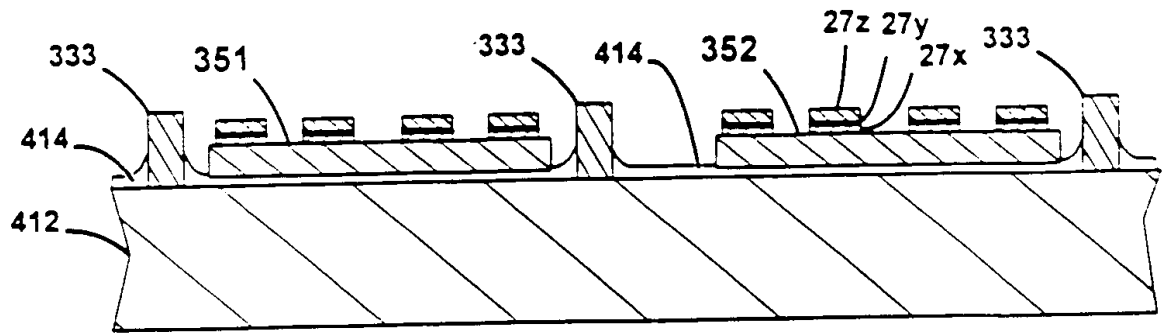


FIG. 39

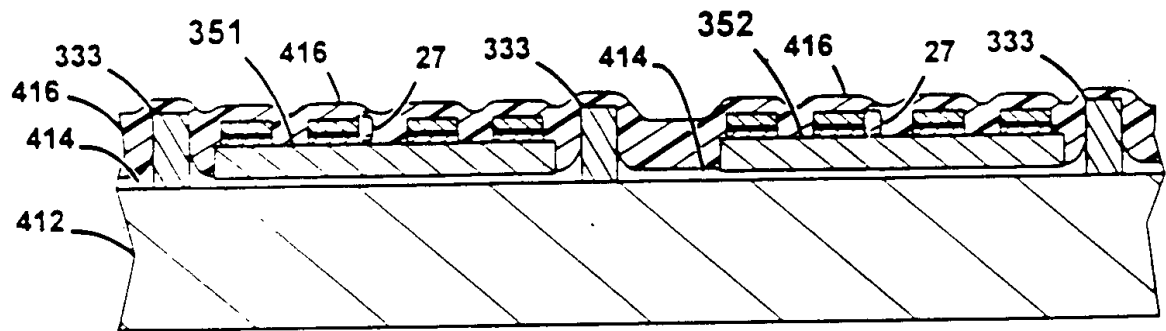


FIG. 40

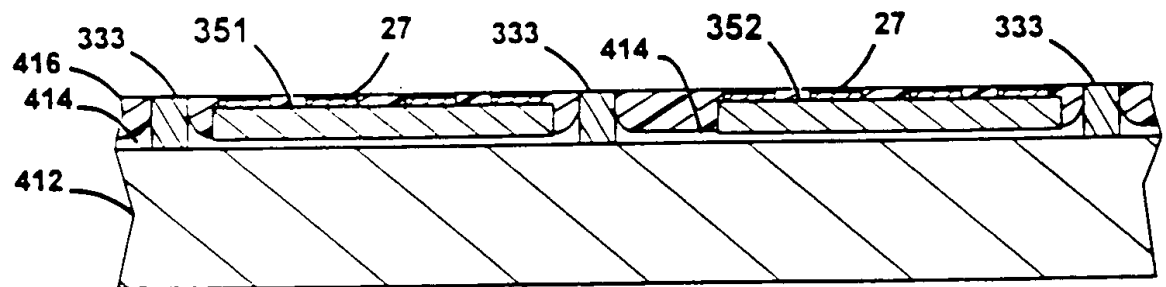


FIG. 41

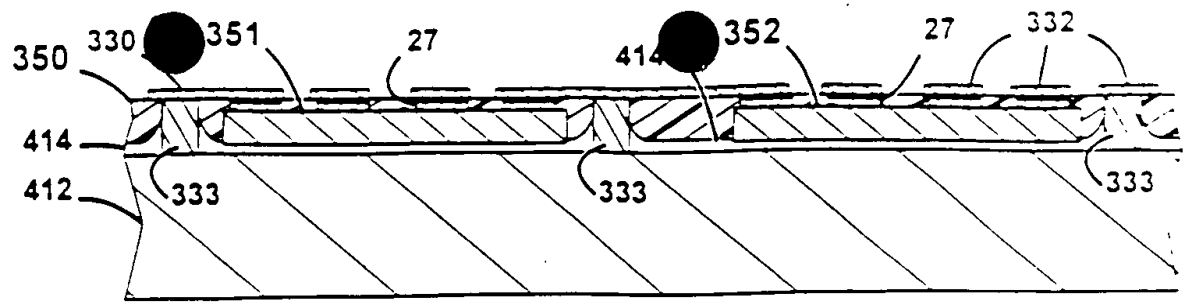


FIG. 42

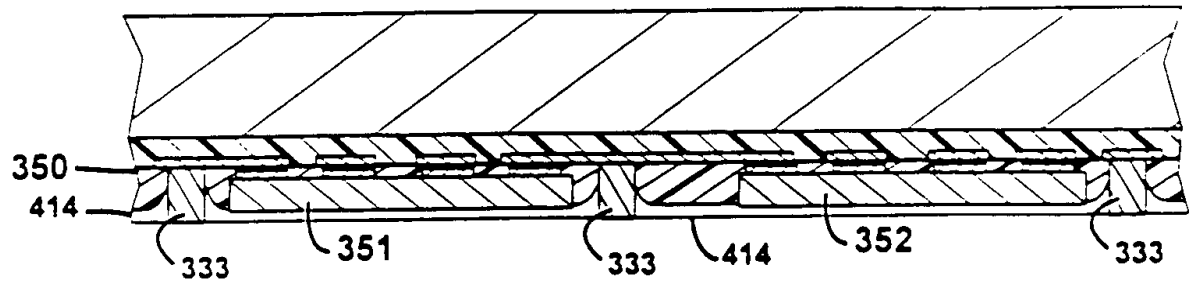


FIG. 43

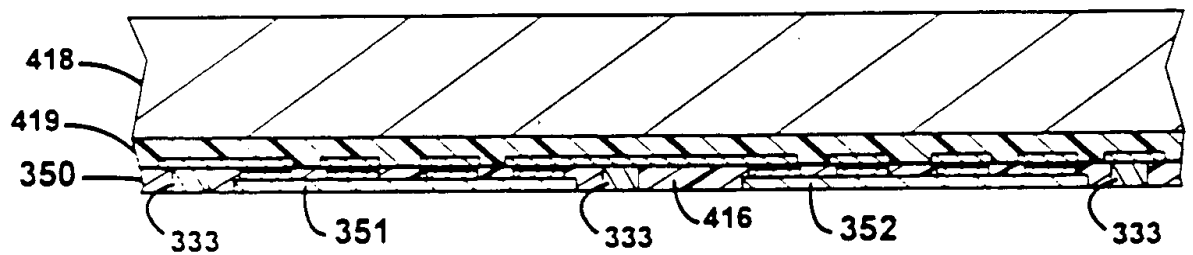


FIG. 44

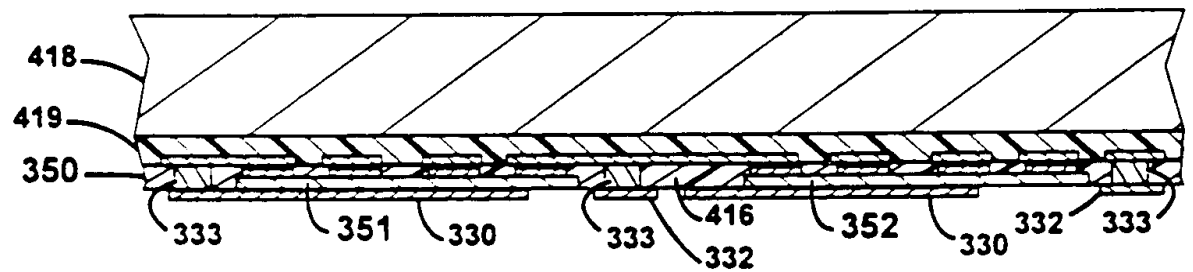


FIG. 45

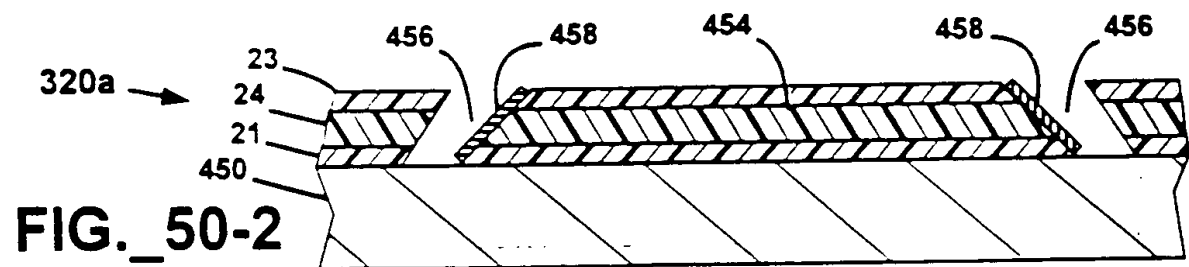
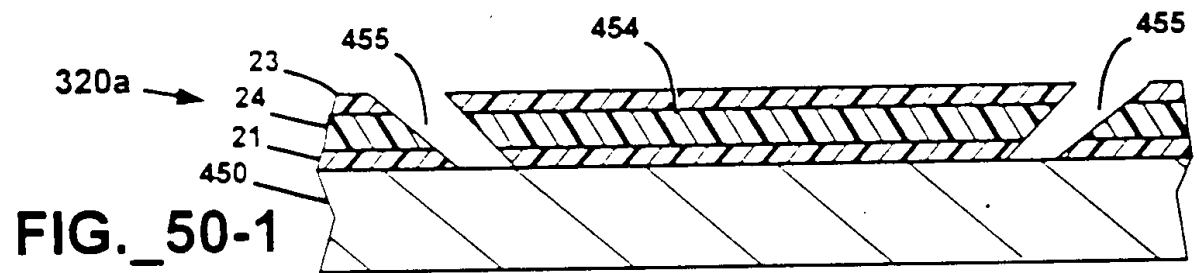
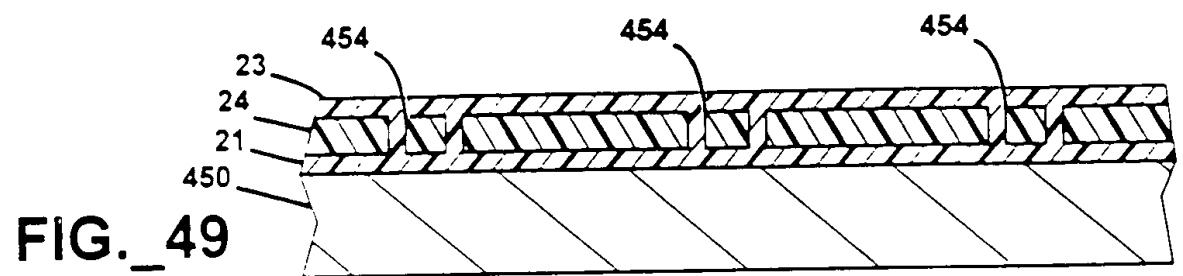
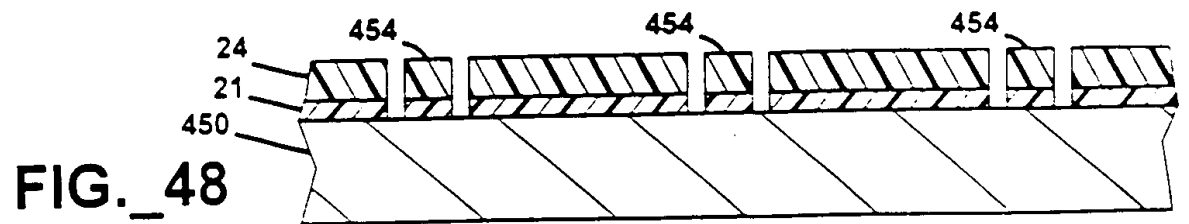
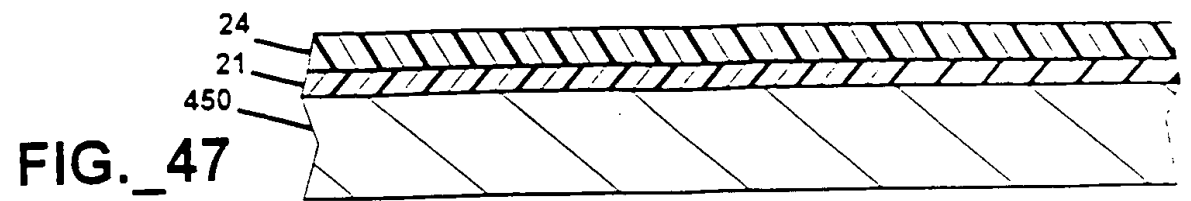
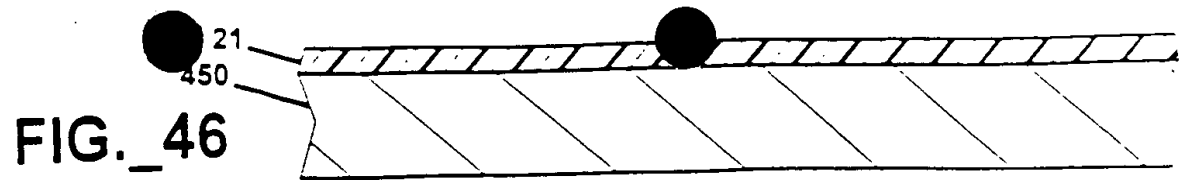


FIG._54

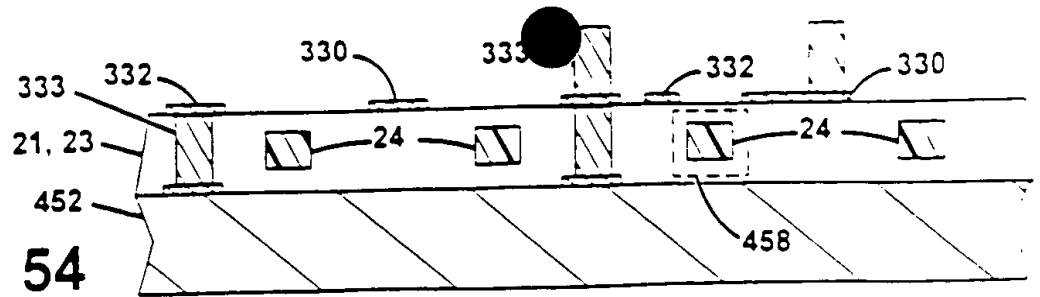


FIG._55

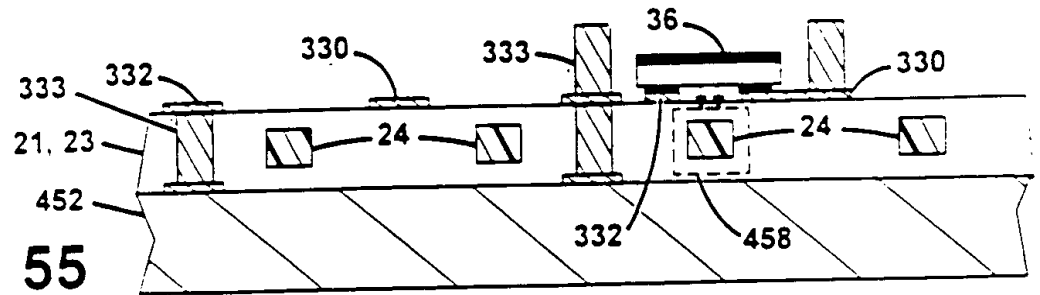


FIG._56

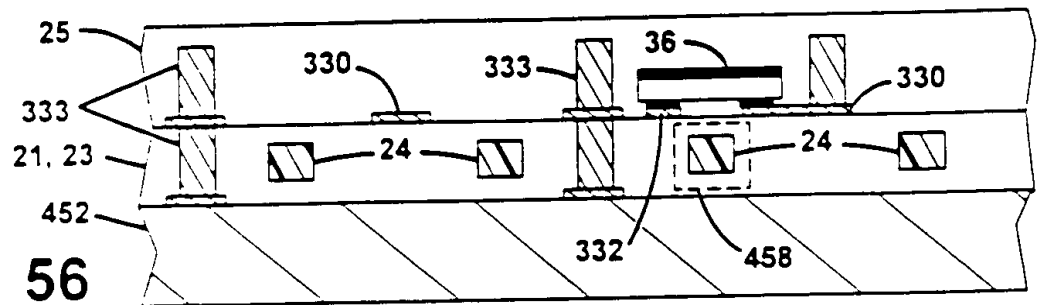


FIG._57

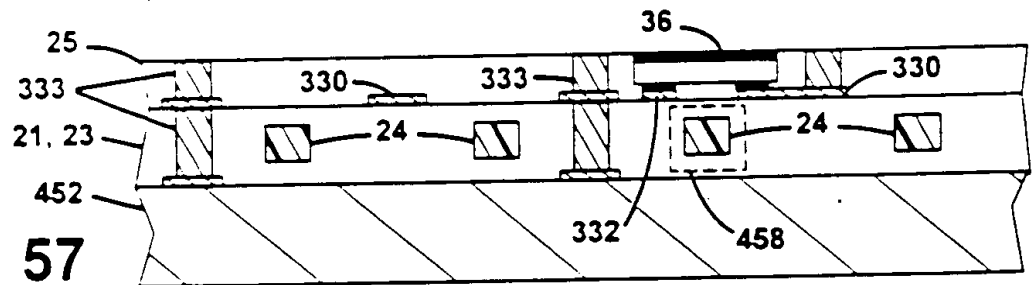
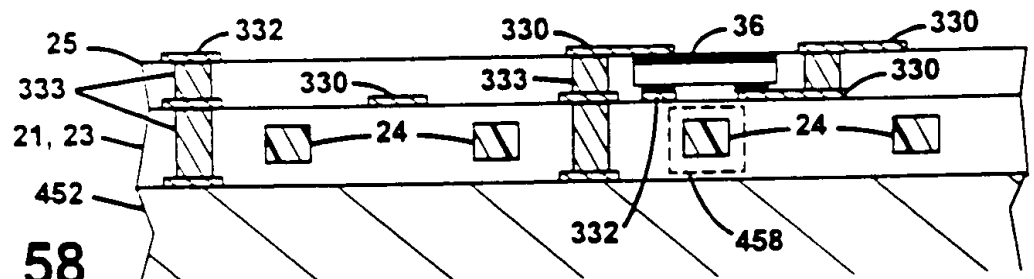


FIG. 58



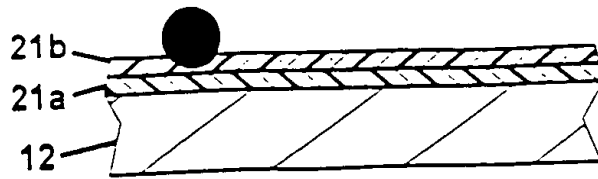


FIG._59

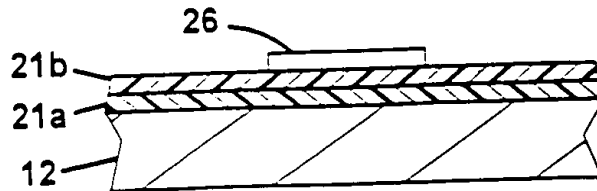


FIG._60

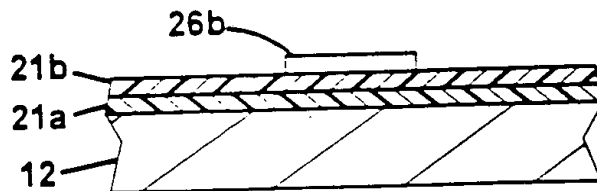


FIG._62

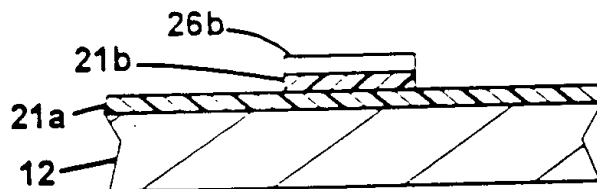


FIG._64

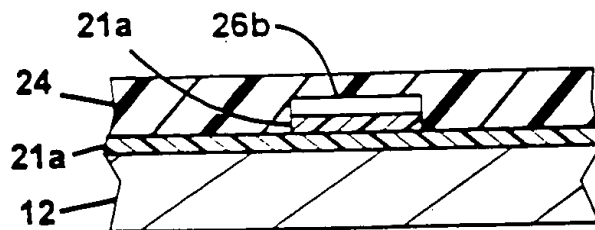


FIG._65

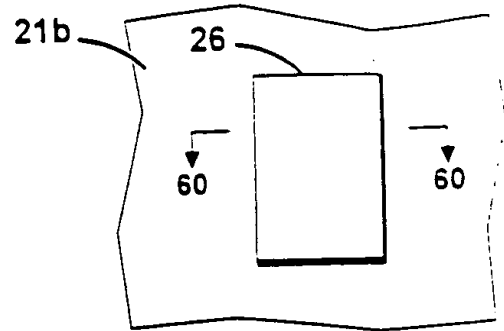


FIG._61

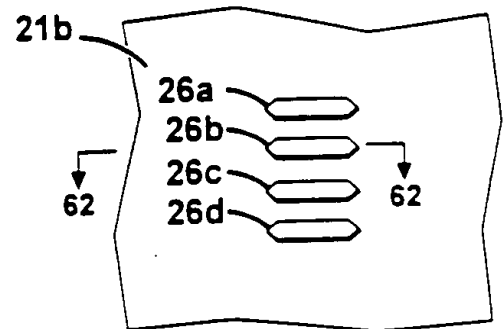


FIG._63

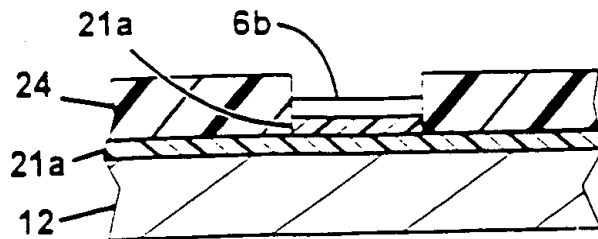


FIG. 66

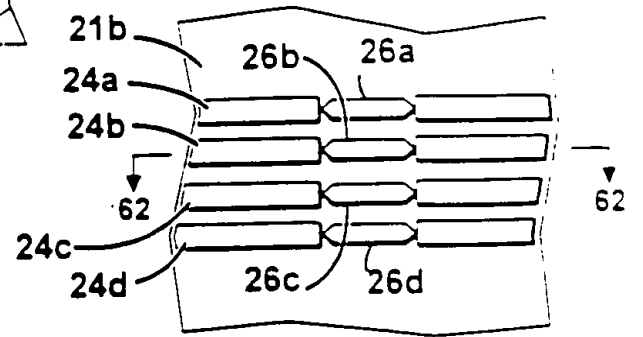


FIG. 67

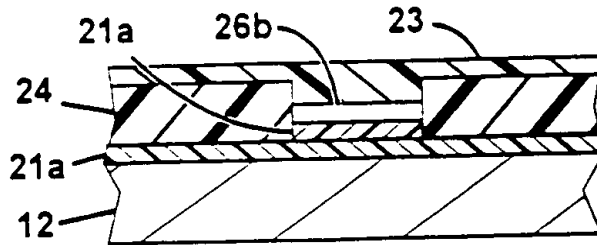


FIG. 68

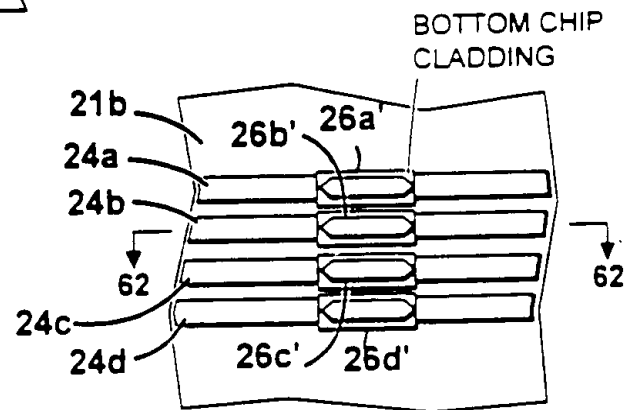
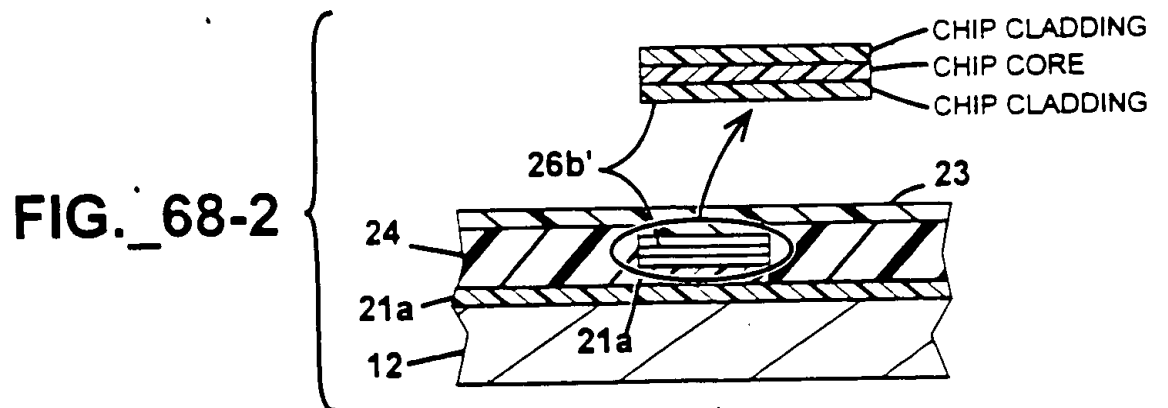


FIG. 67-2



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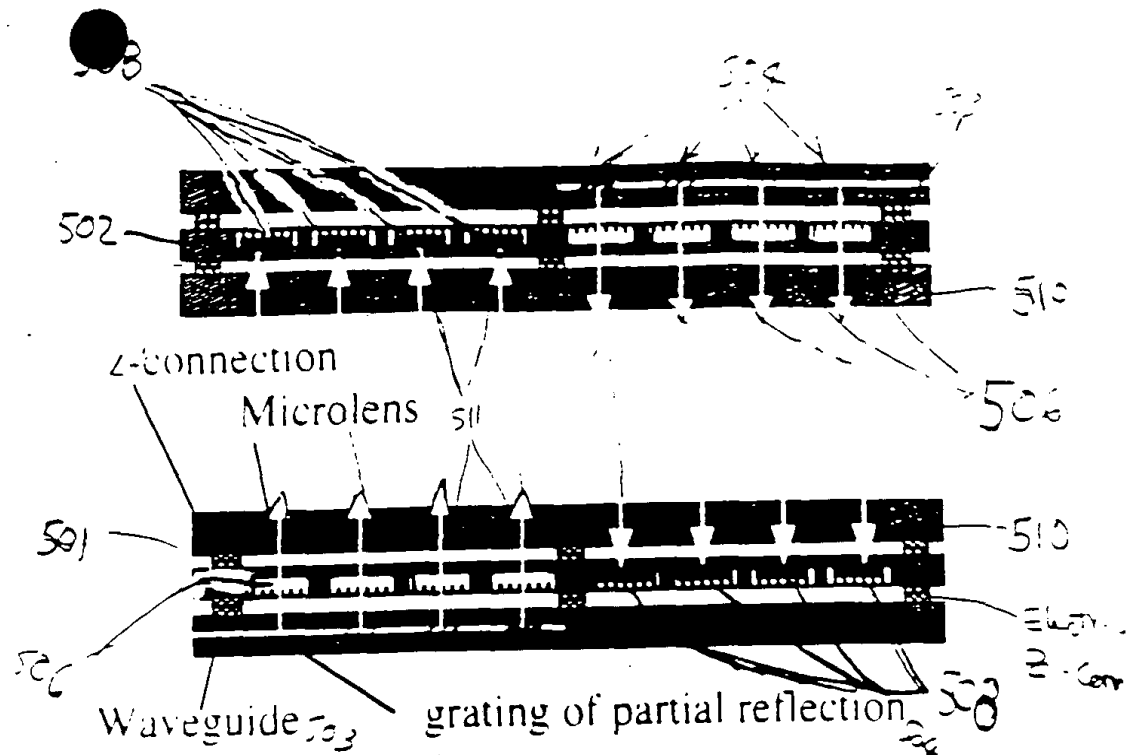


FIG. 69

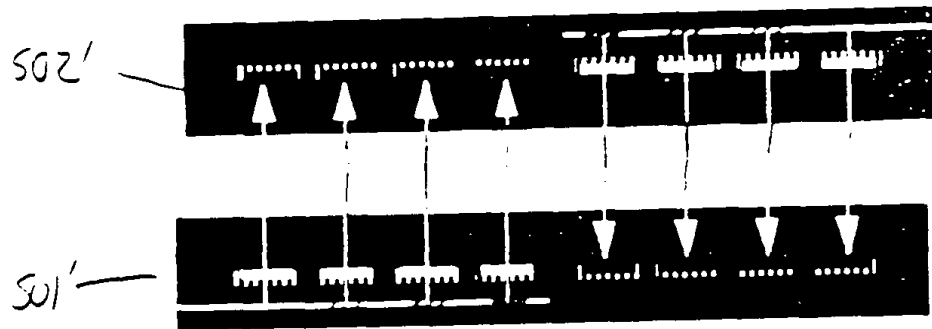


FIG. 70

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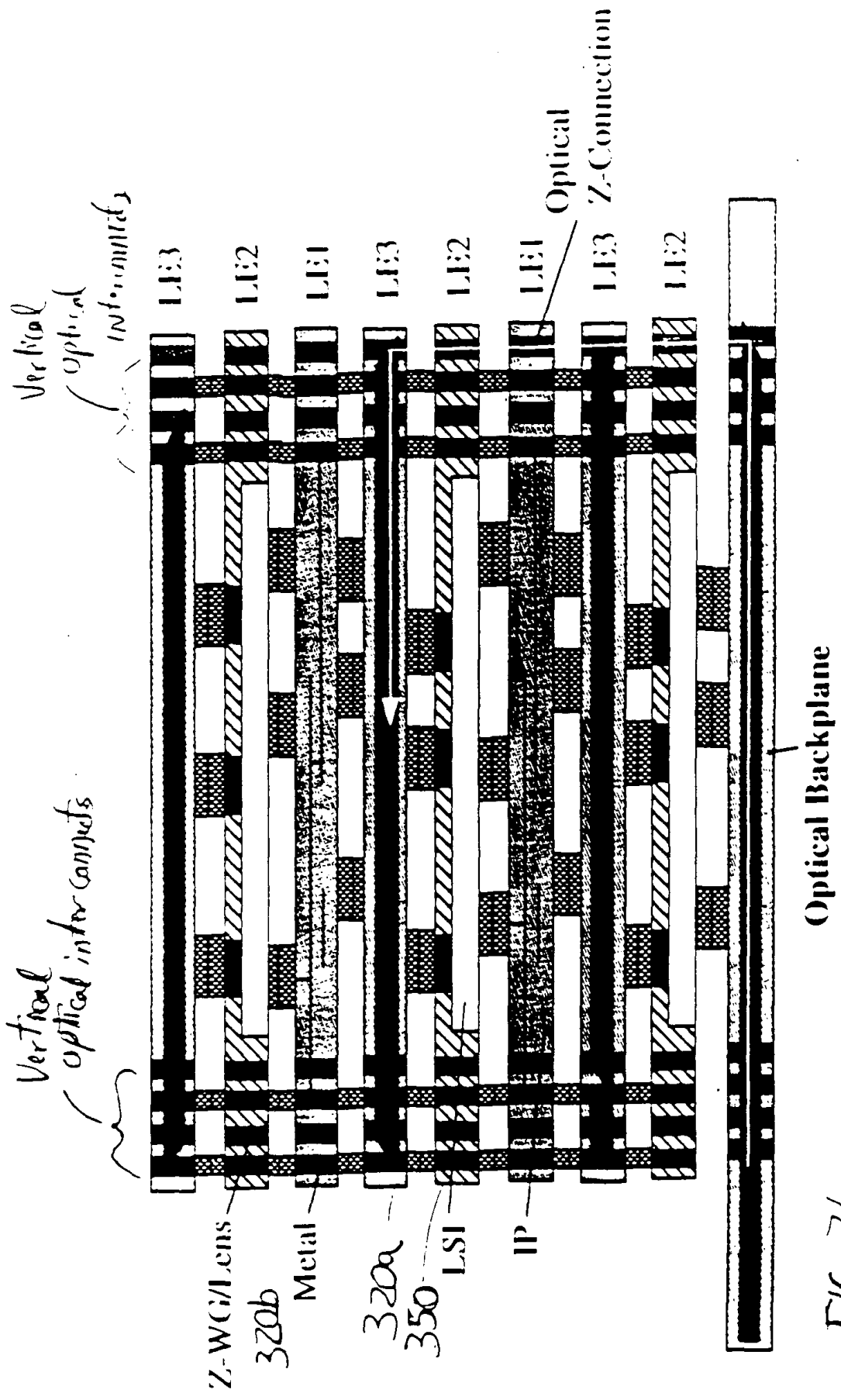
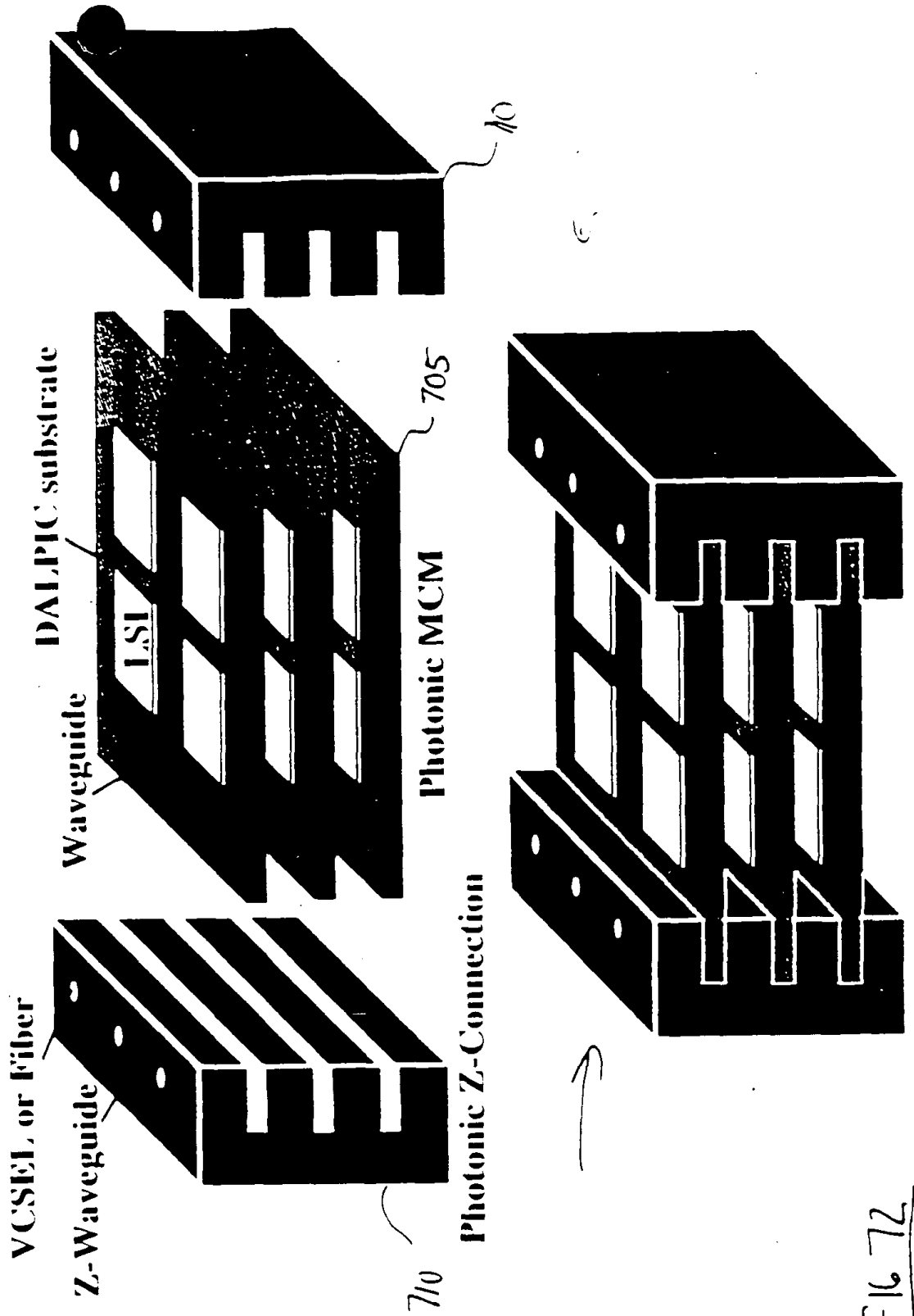
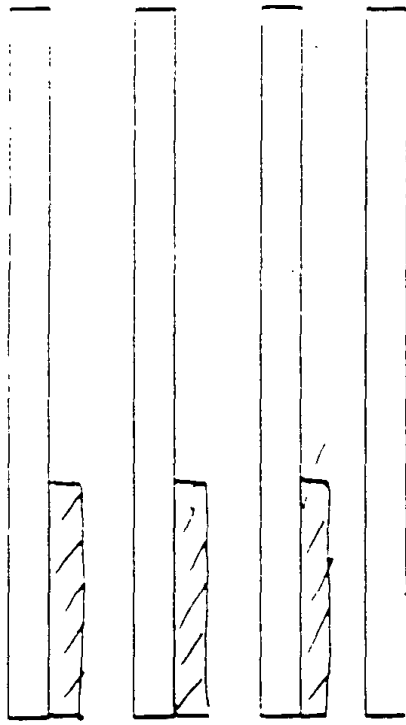
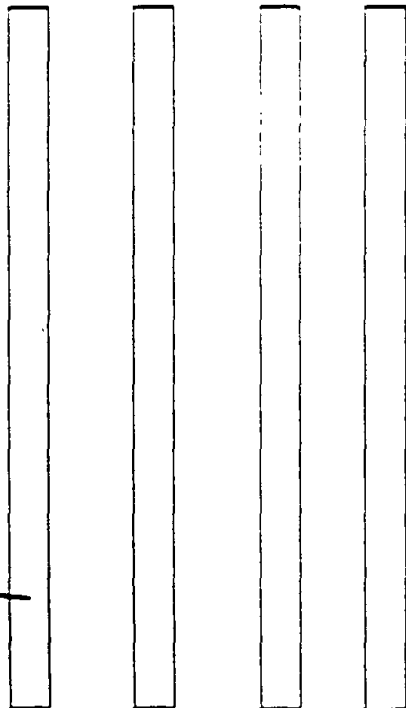


FIG. 71



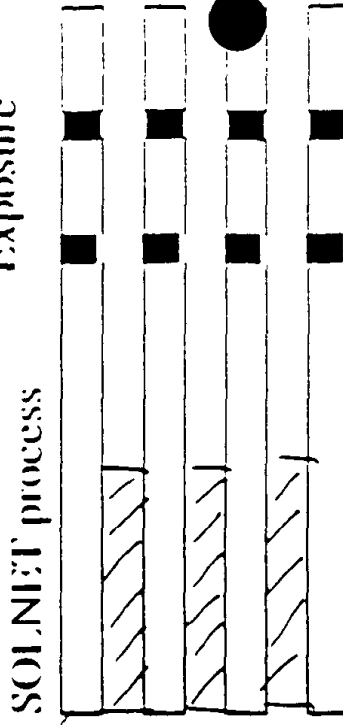
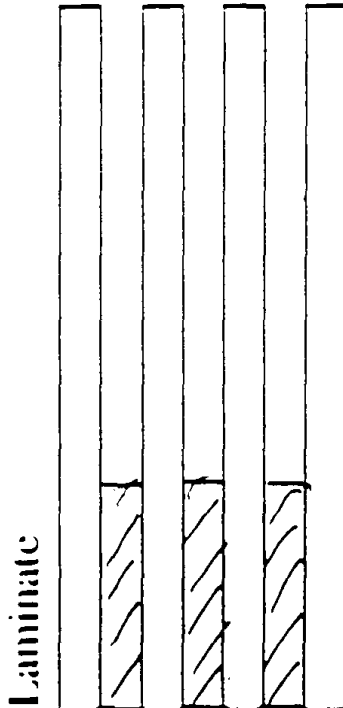
Flexible Photo-imagable sheet (Polyguide)

Bonding sheet attach

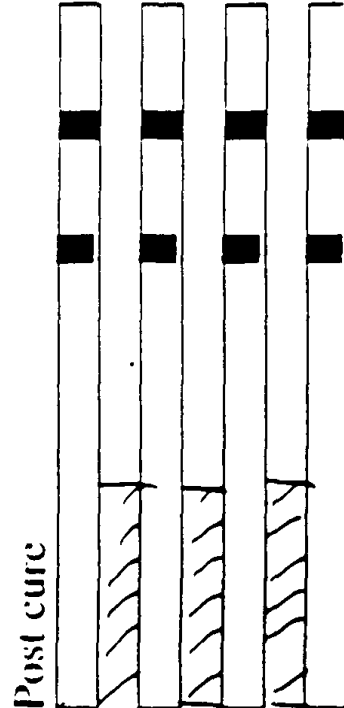


Exposure

SOLNET process



Post cure



Assemble

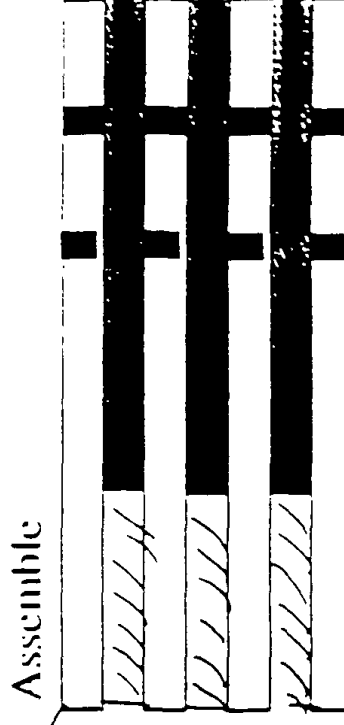


FIG. 73

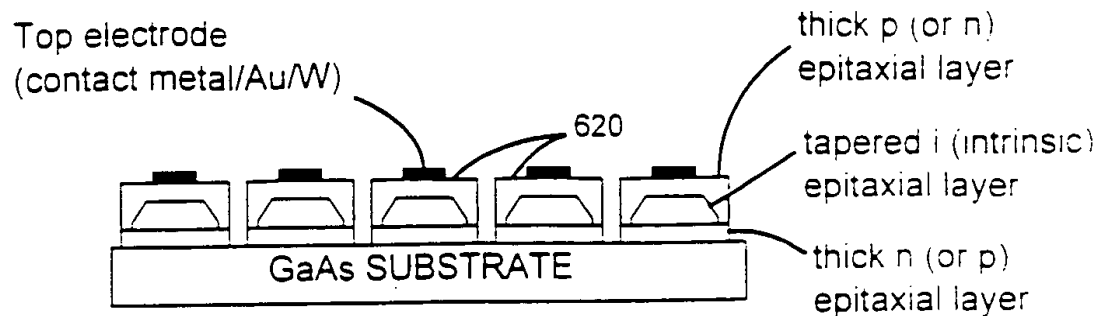


FIG._74 (Epitaxial growth and patterning)

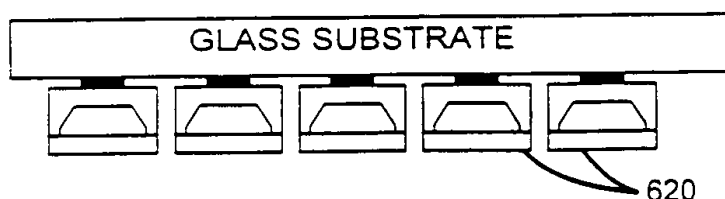


FIG._75 (Epitaxial liftoff)

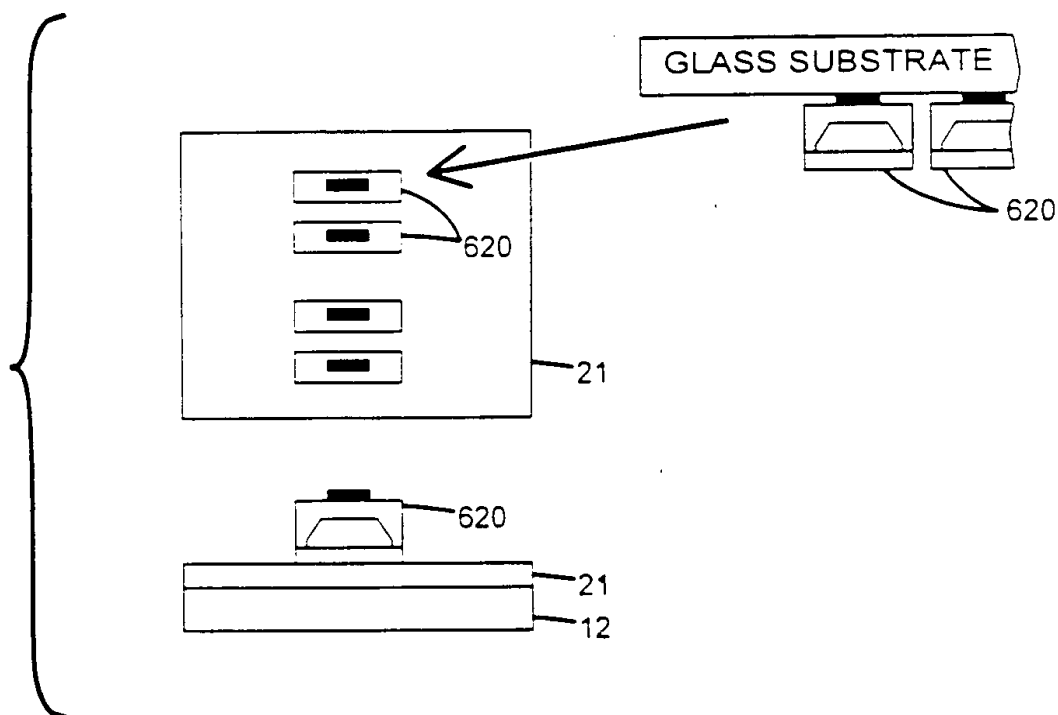
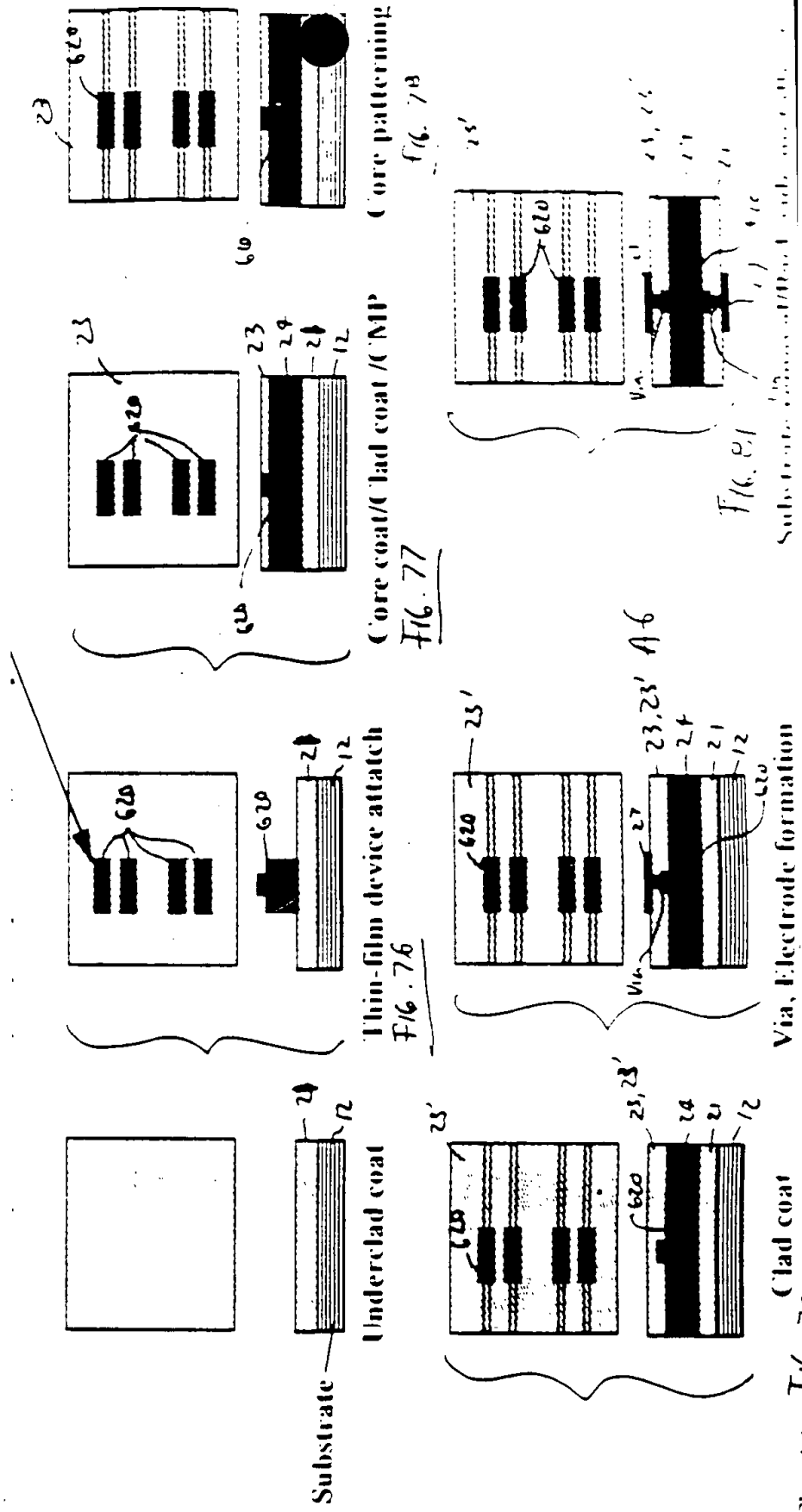


FIG._76 (Transfer)



Substrate, Underclad coat, Thin-film device attach, Core coat, Clad coat

FIG. 82

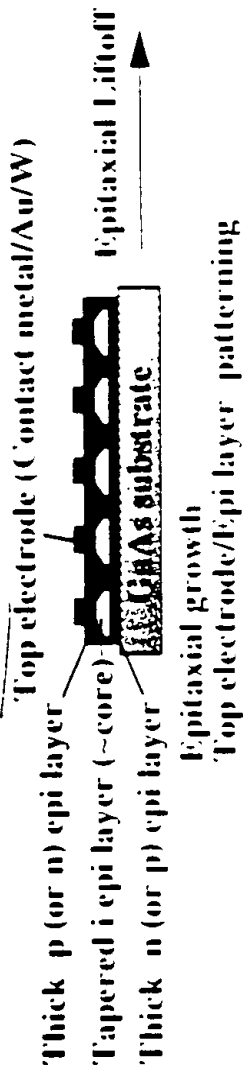


FIG. 84

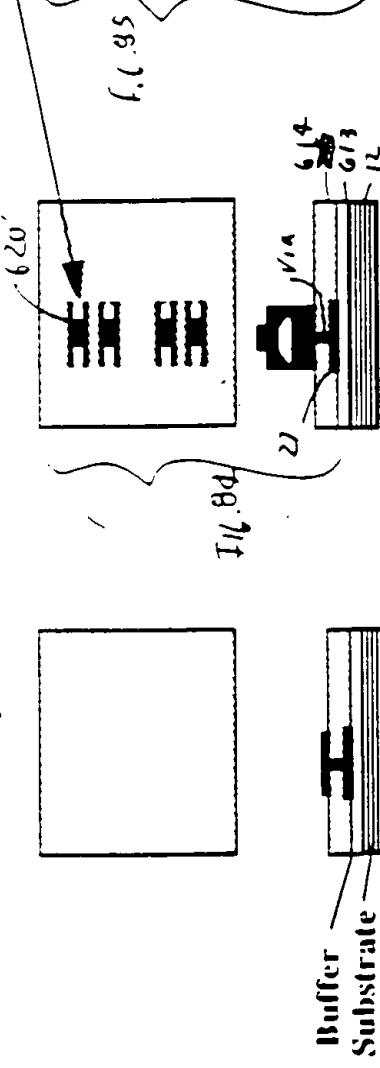


FIG. 85

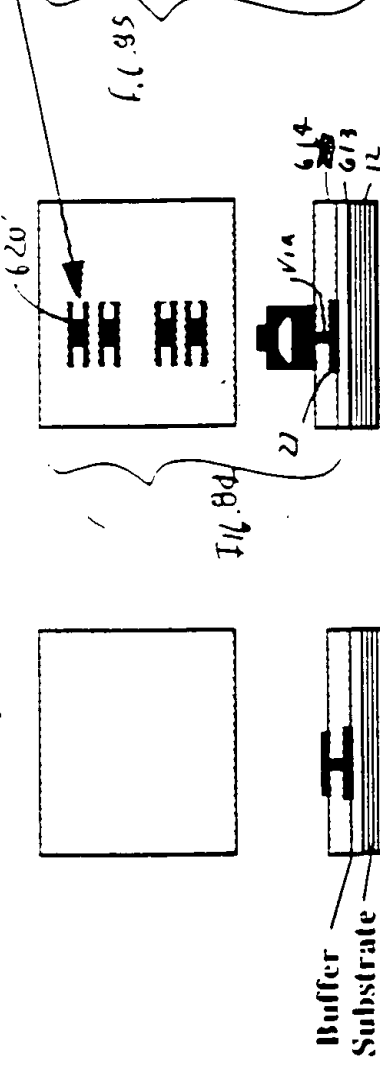


FIG. 86

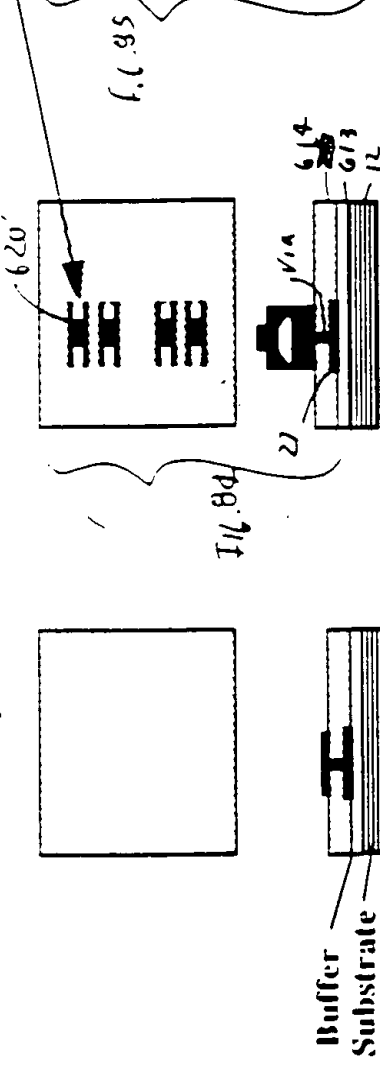


FIG. 87

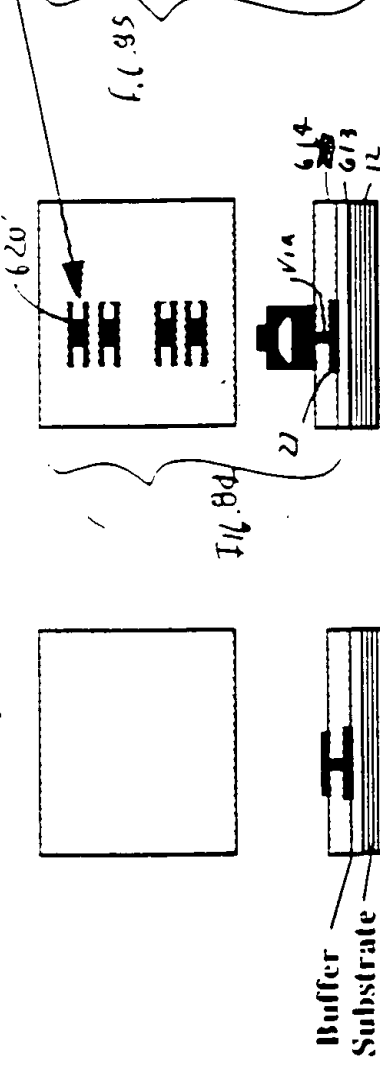


FIG. 88

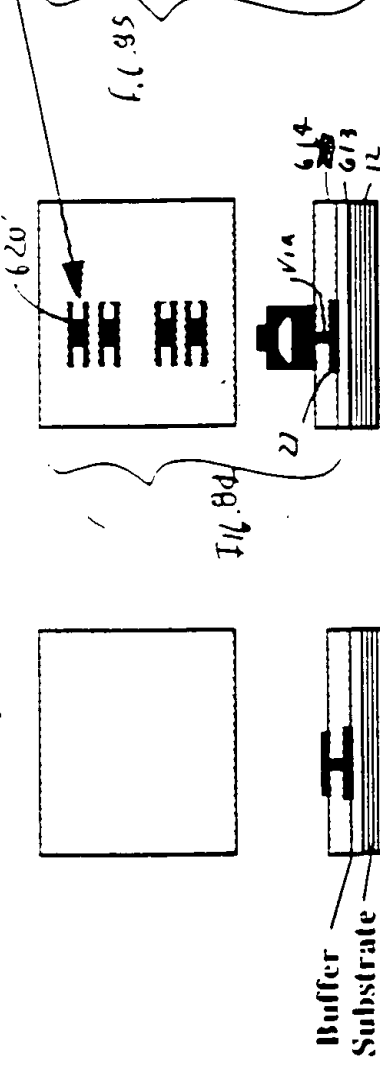


FIG. 89

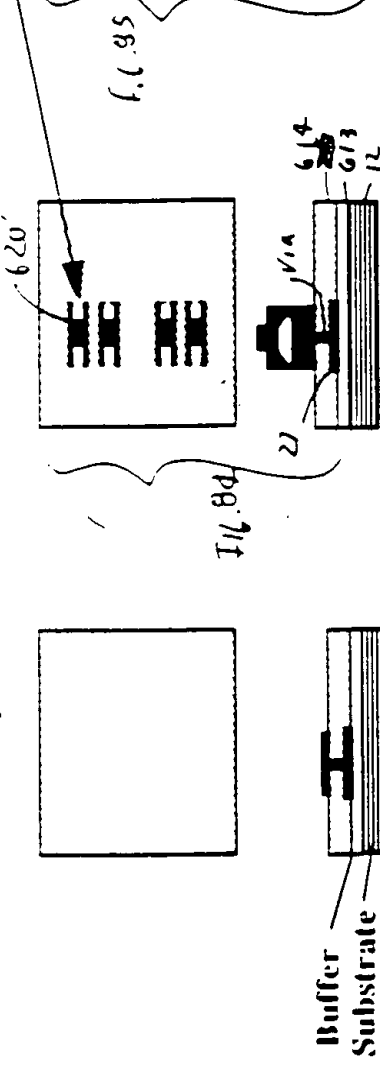


FIG. 90

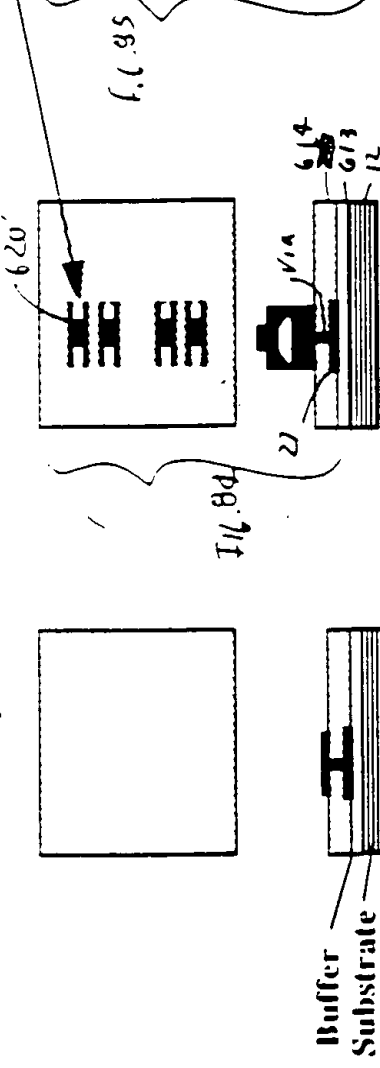


FIG. 91

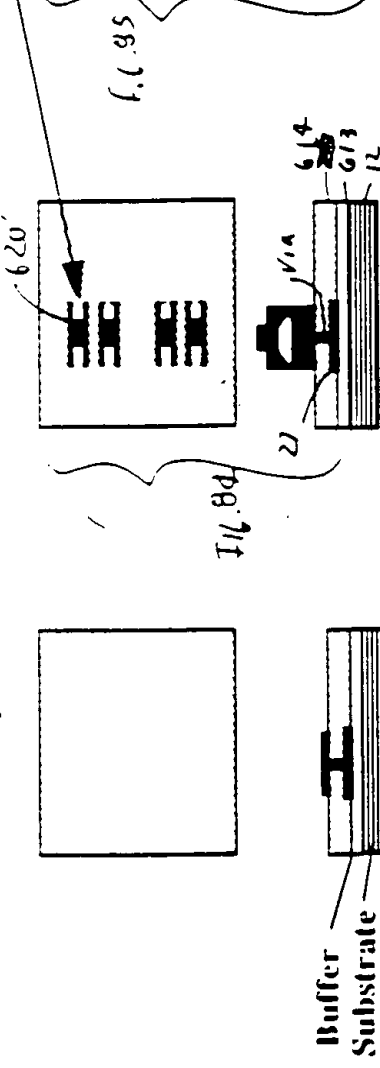


FIG. 92

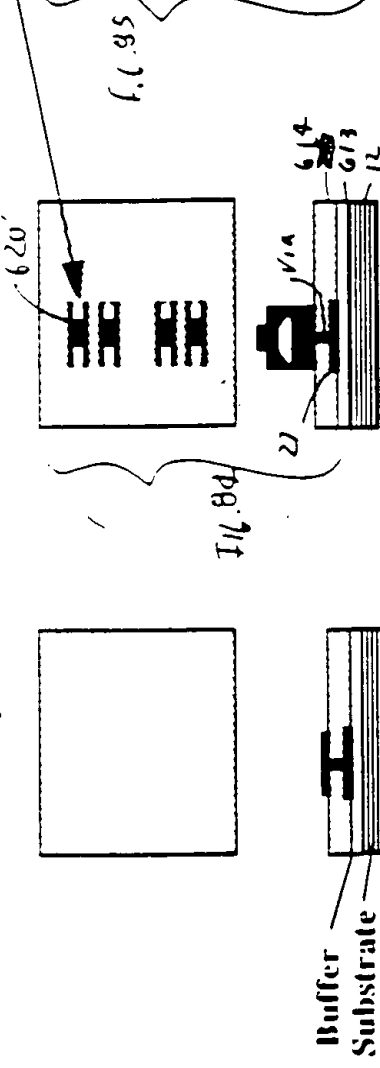


FIG. 93

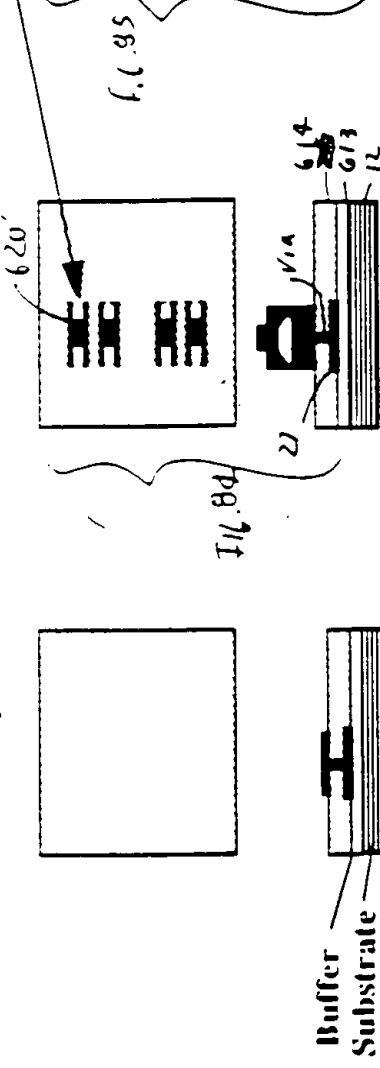


FIG. 94

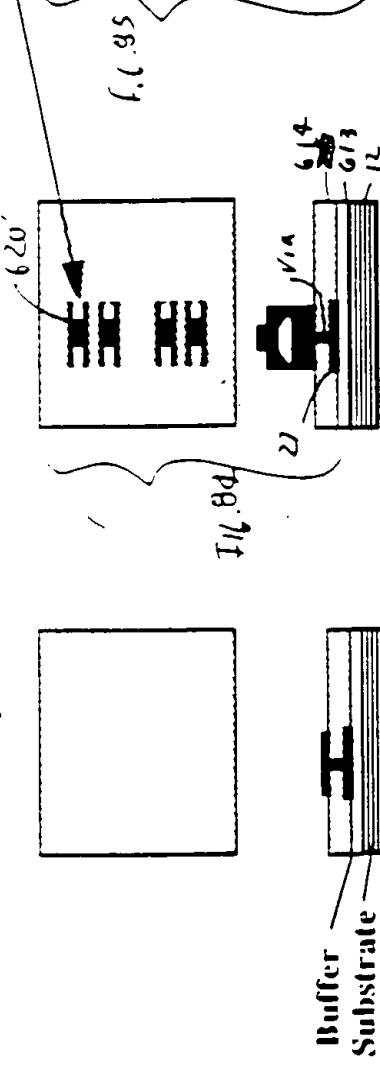


FIG. 95

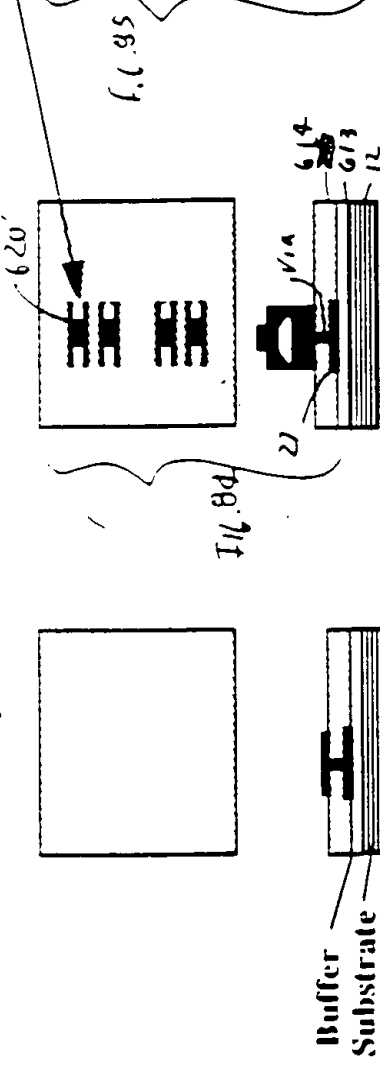


FIG. 96

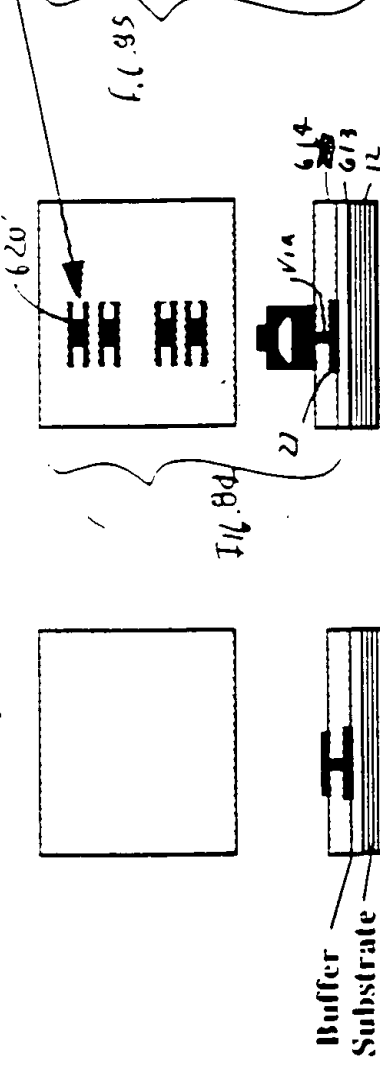


FIG. 97

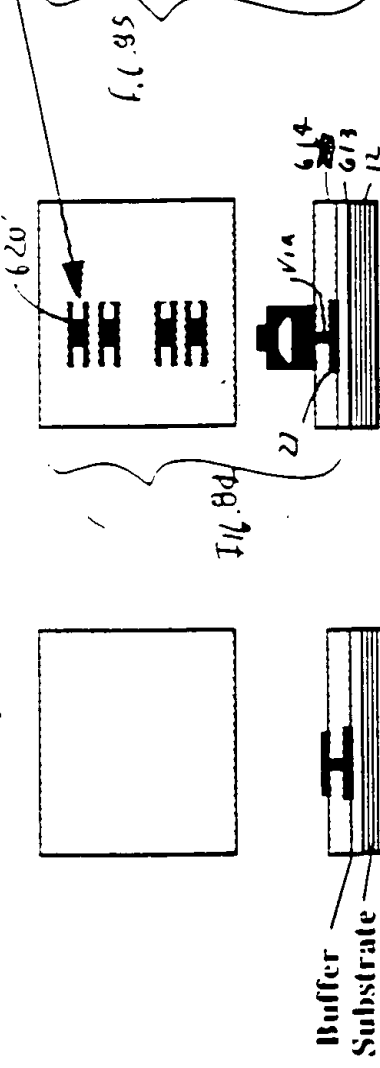


FIG. 98

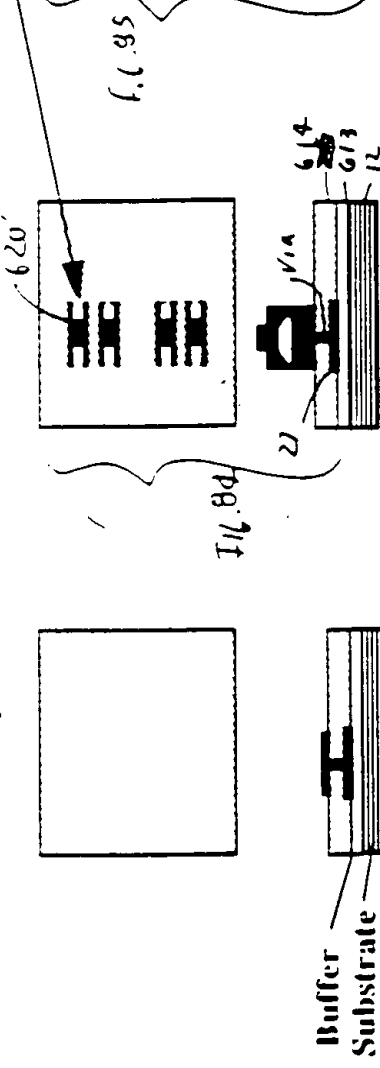


FIG. 99

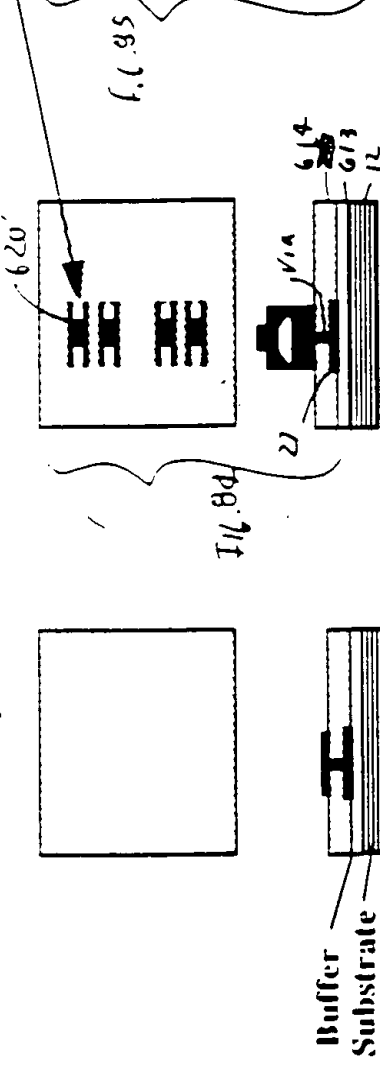


FIG. 100

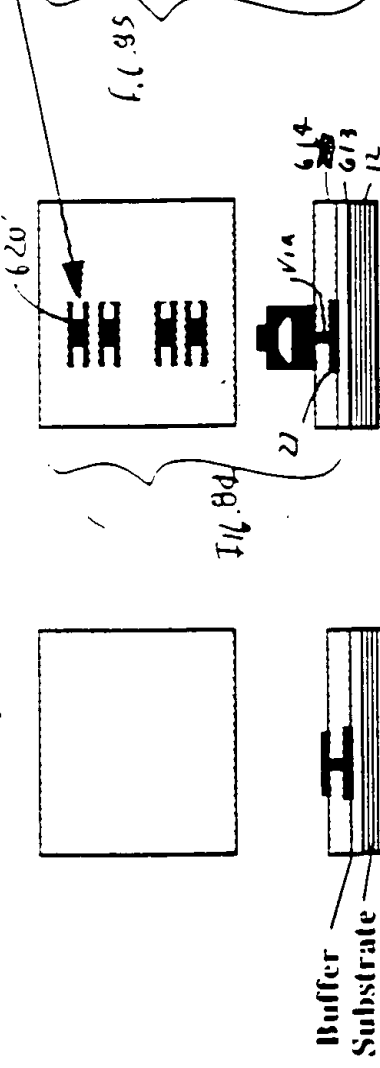


FIG. 101

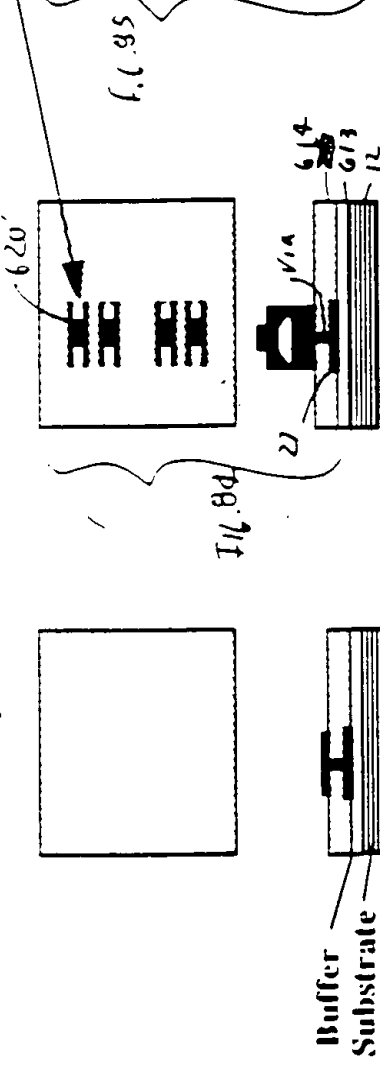


FIG. 102

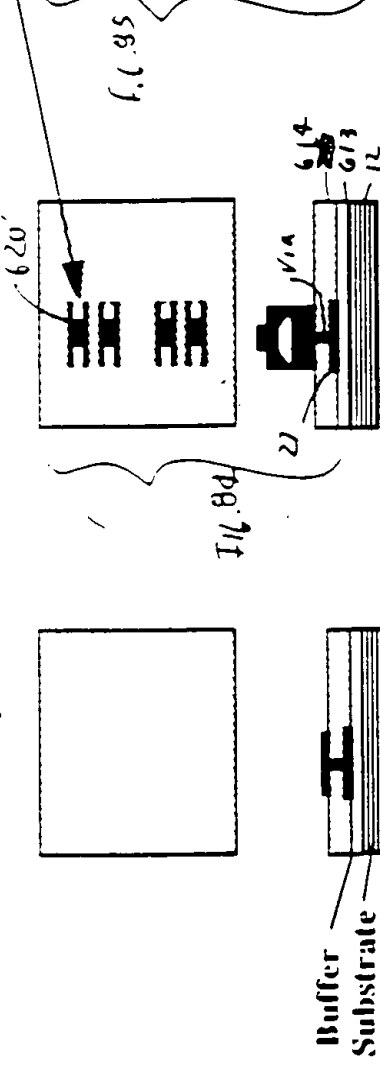


FIG. 103

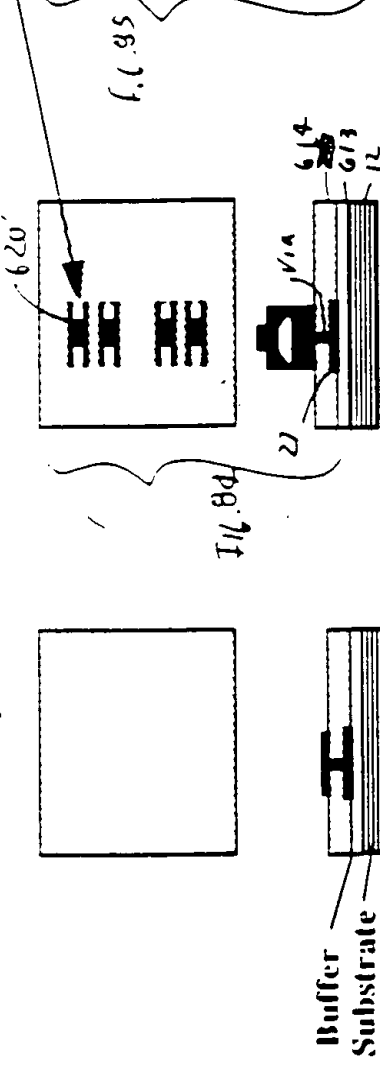


FIG. 104

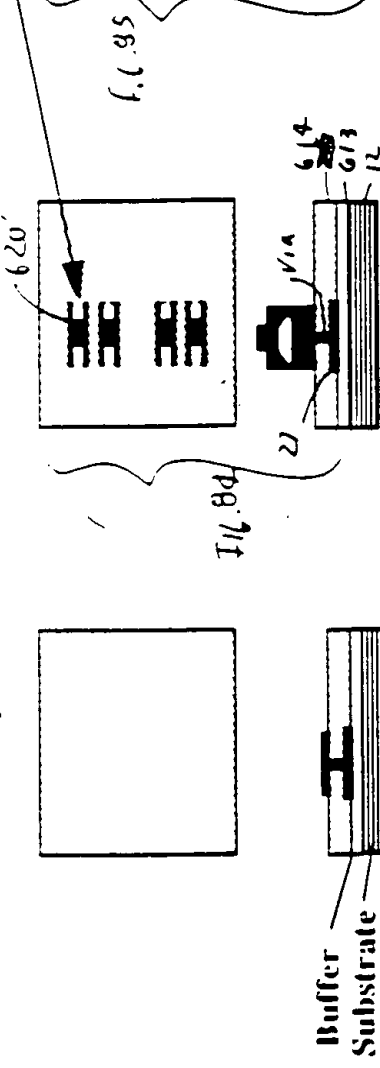


FIG. 105

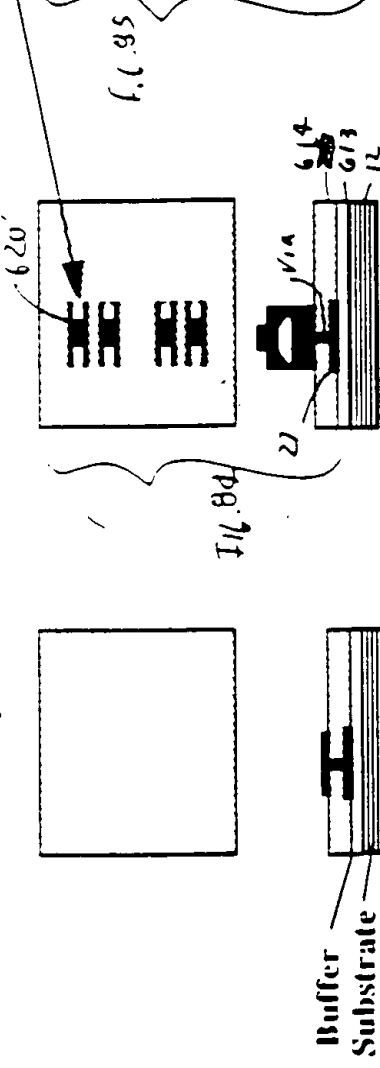


FIG. 106

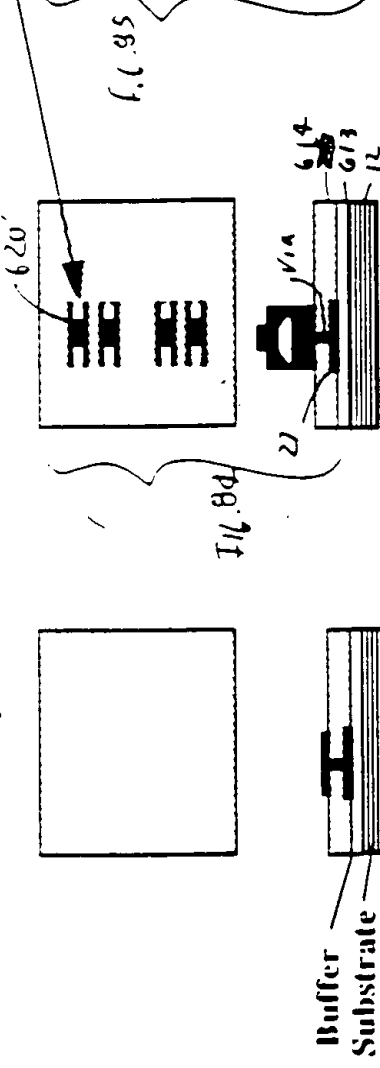


FIG. 107

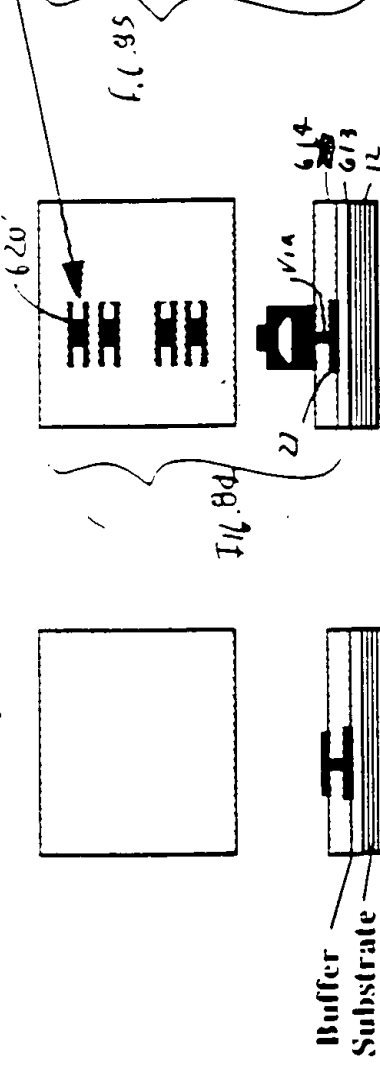


FIG. 108

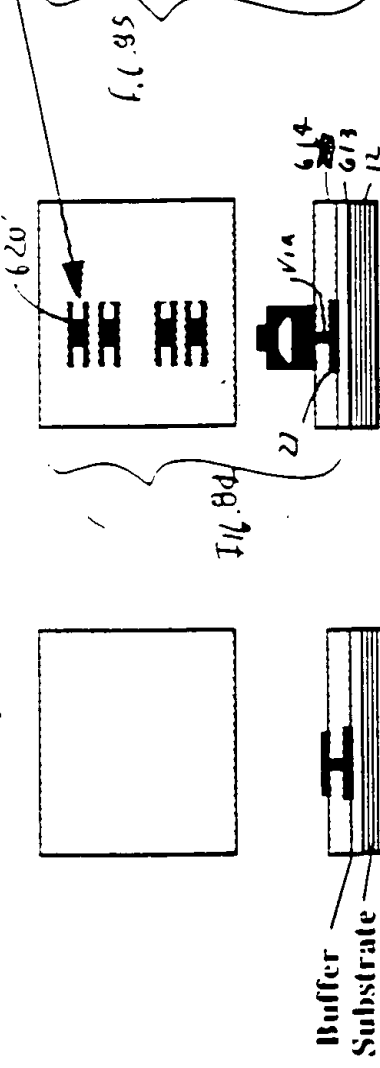


FIG. 109

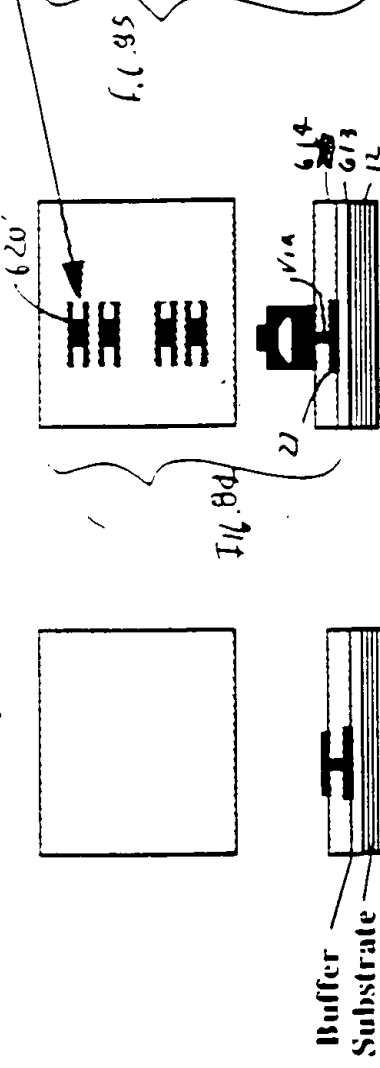


FIG. 110

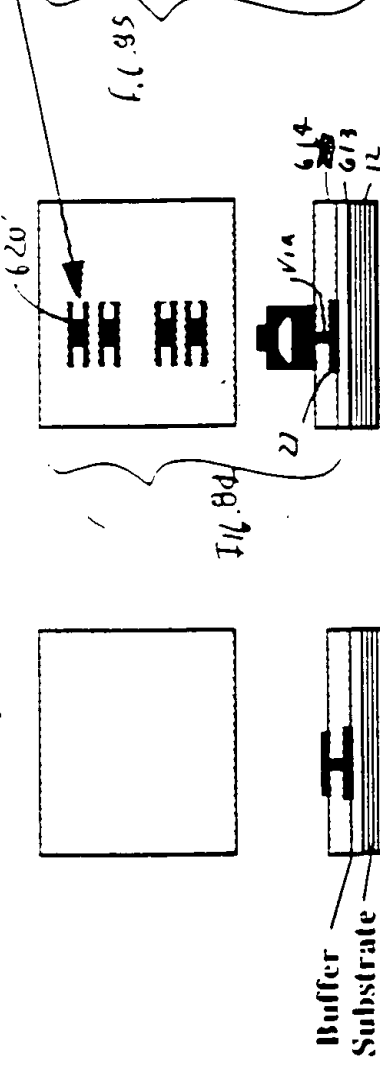


FIG. 111

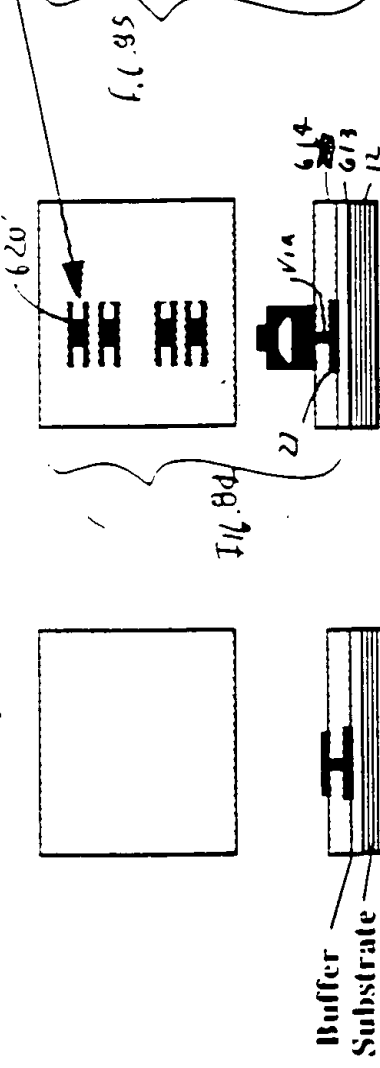


FIG. 112

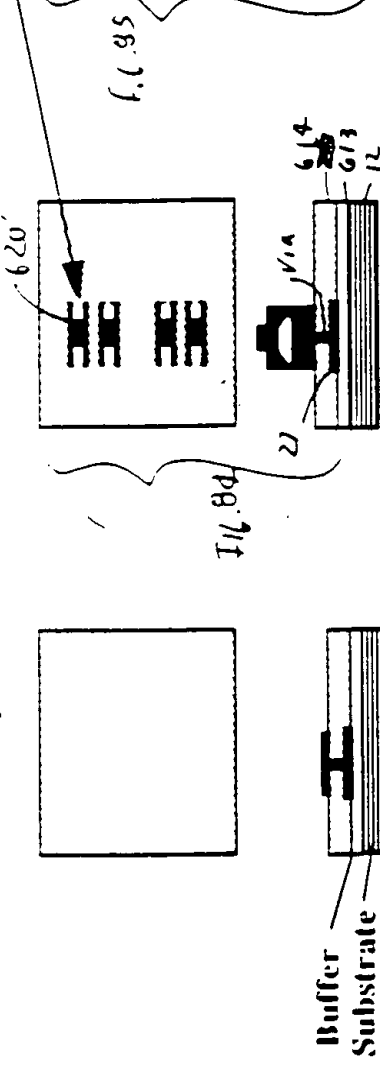


FIG. 113

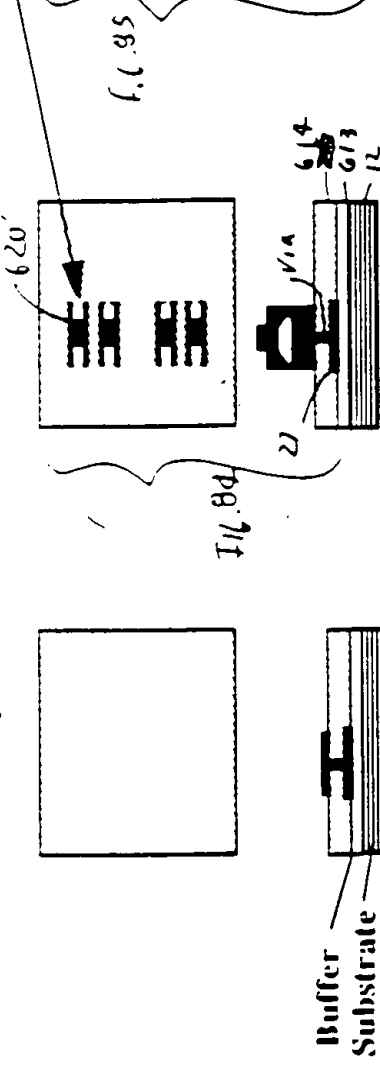


FIG. 114

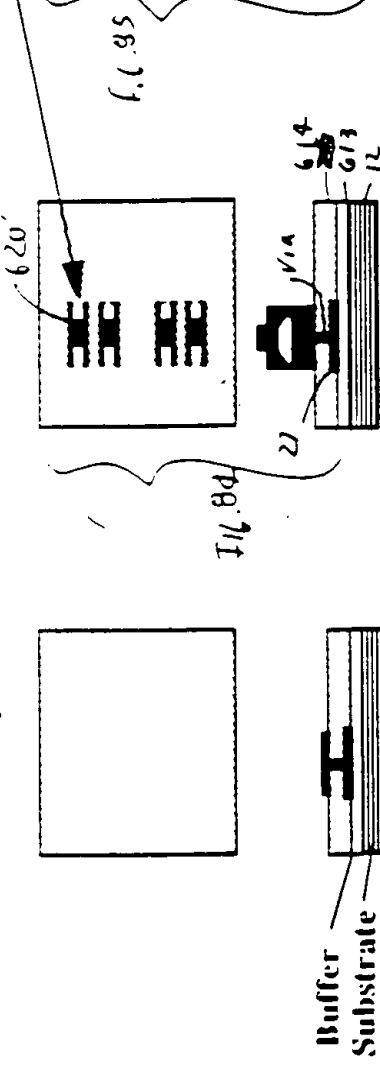


FIG. 115

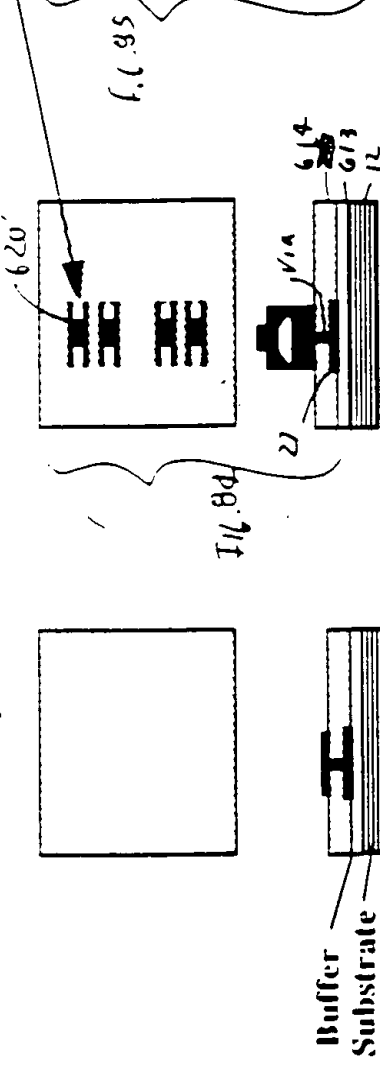


FIG. 116

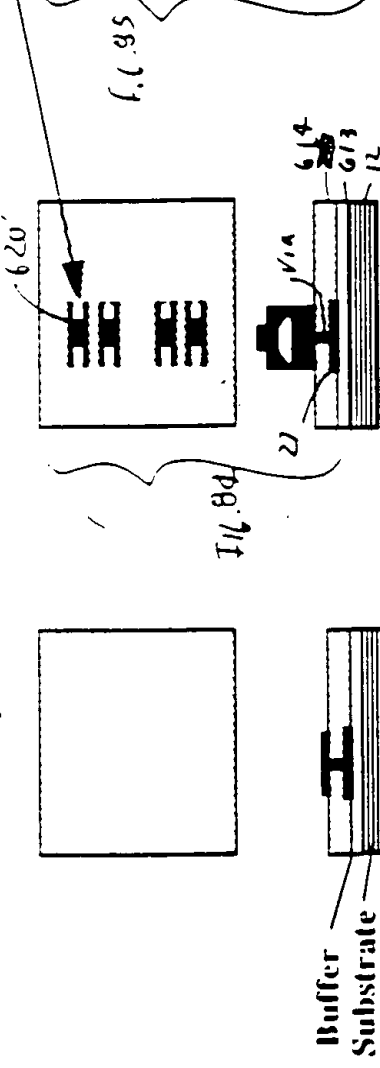


FIG. 117

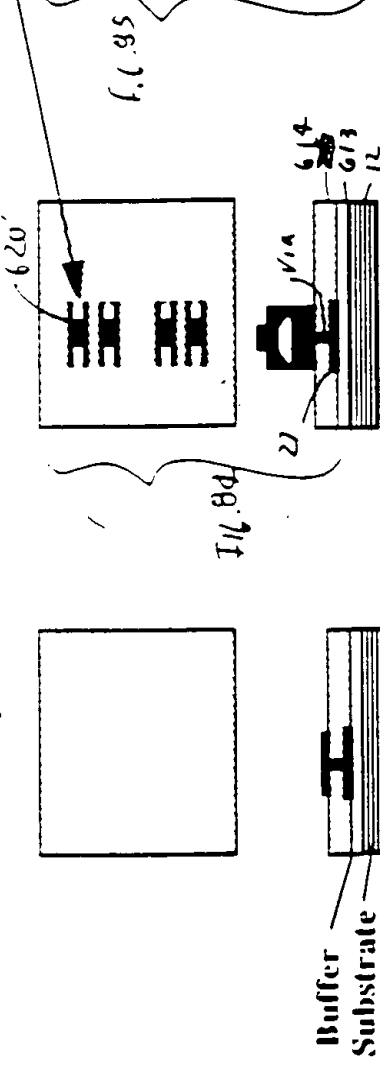


FIG. 118

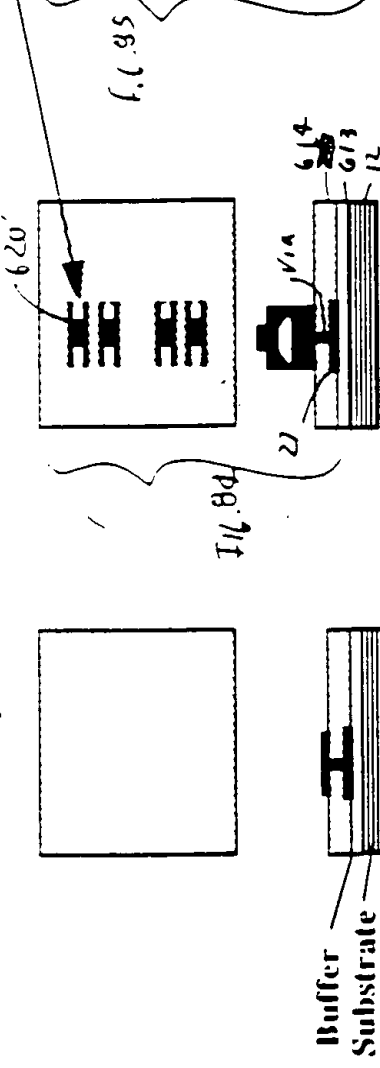


FIG. 119

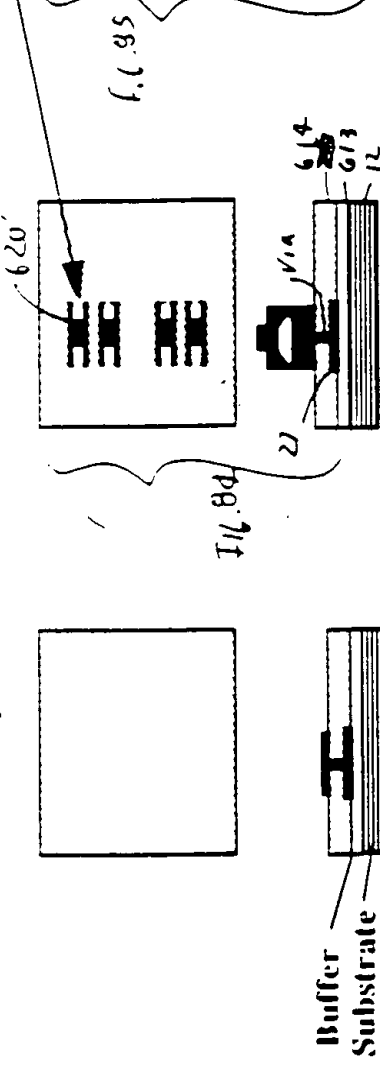


FIG. 120

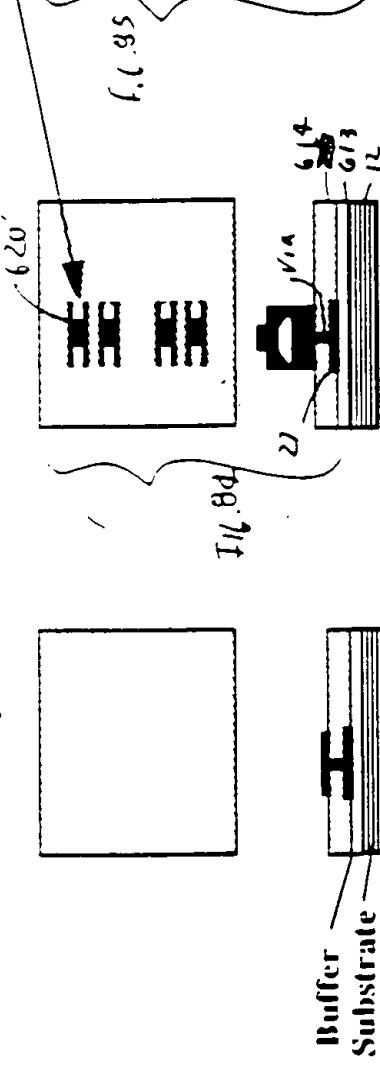


FIG. 121

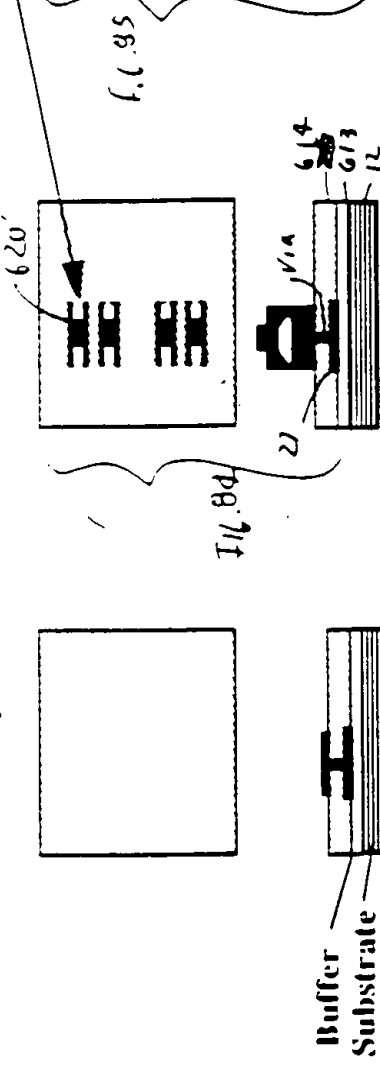


FIG. 122

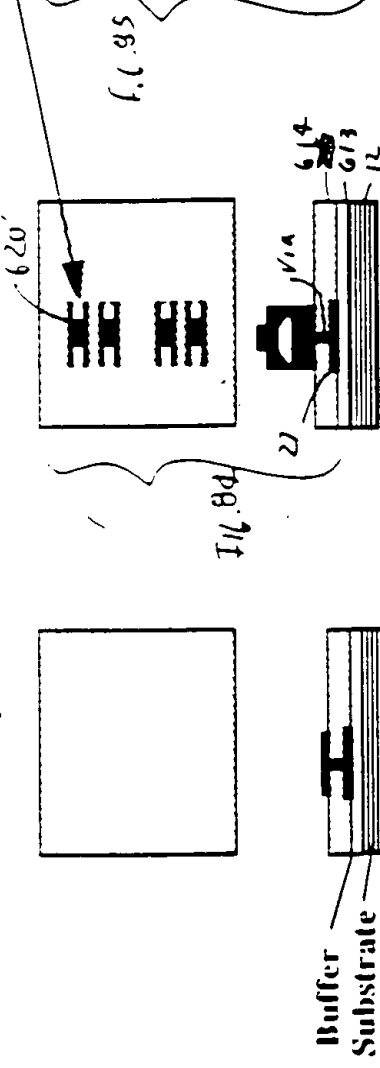


FIG. 123

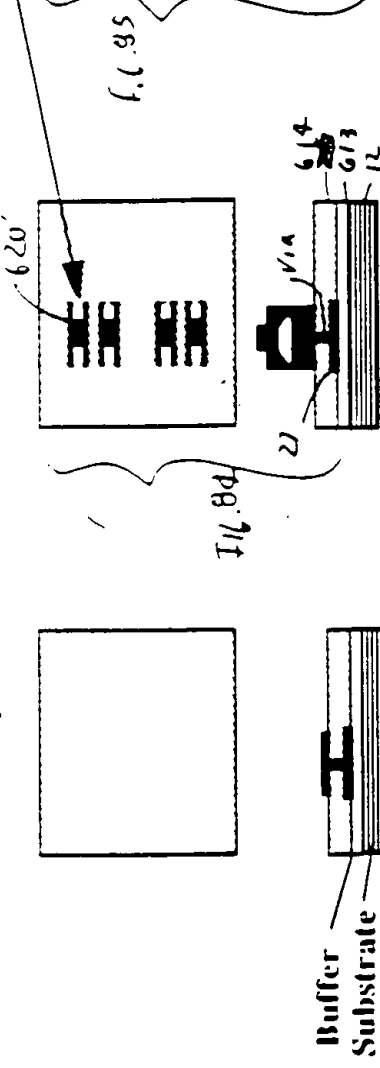


FIG. 124

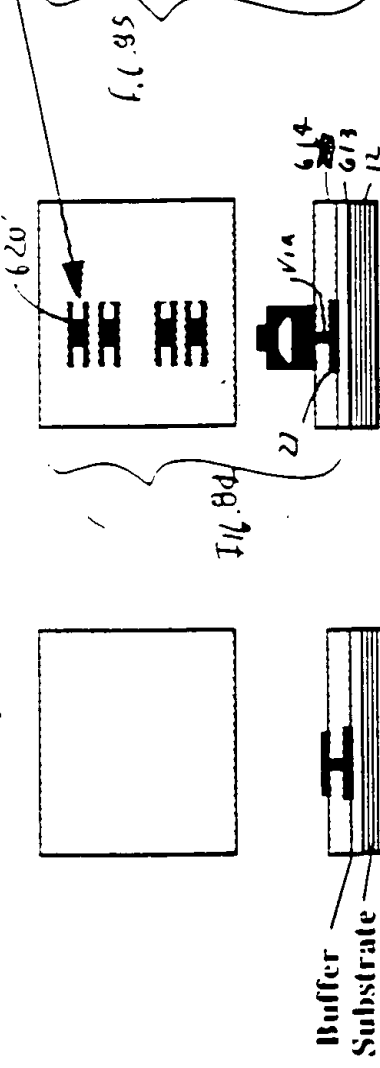


FIG. 125

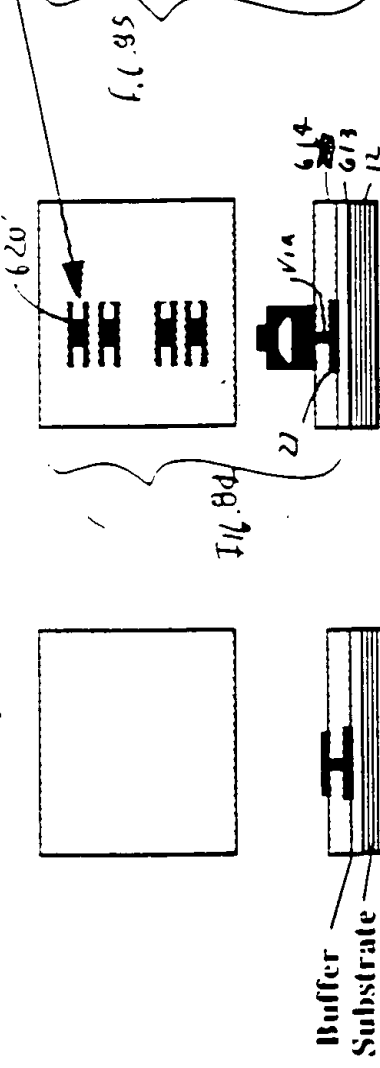


FIG. 126

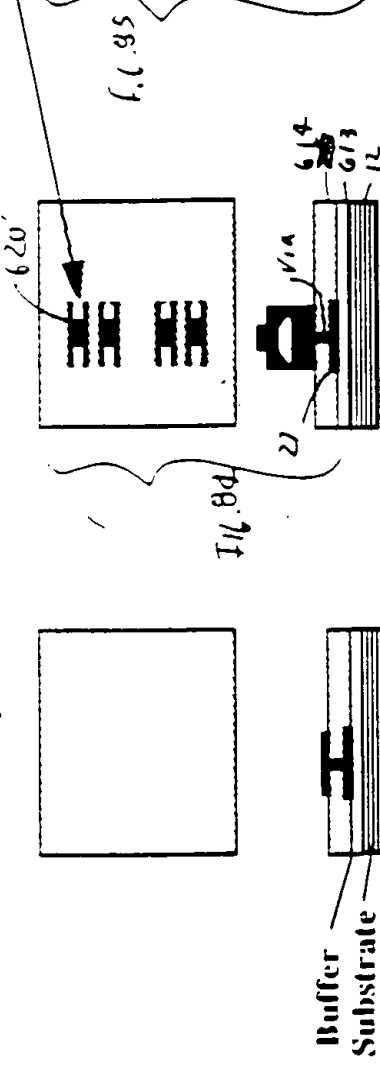


FIG. 127

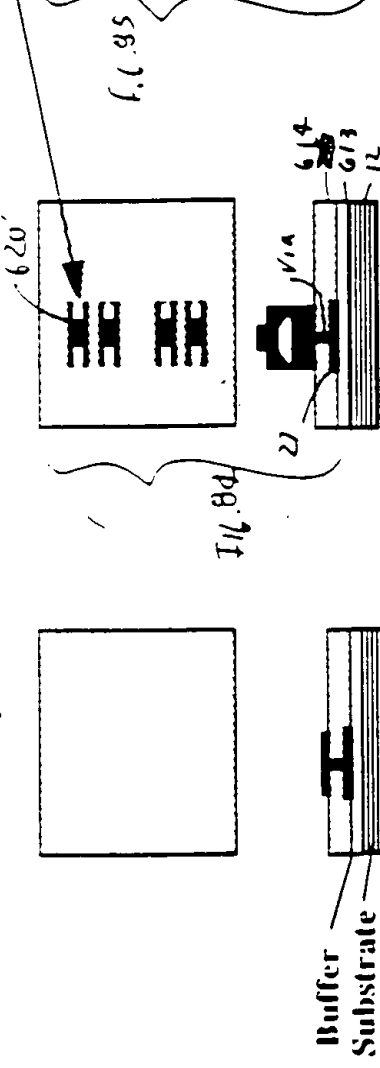


FIG. 128

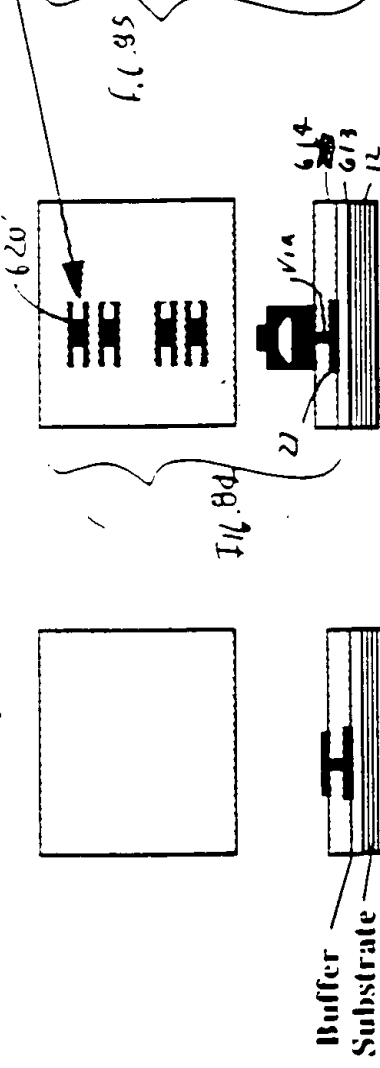


FIG. 129

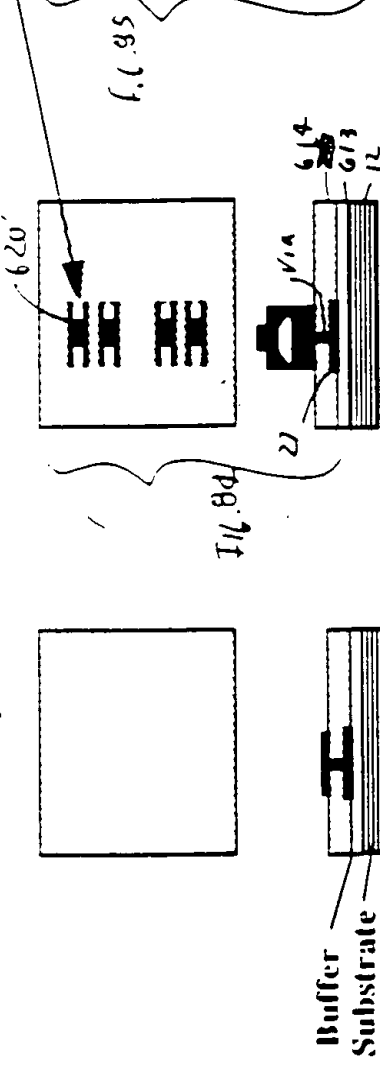


FIG. 130

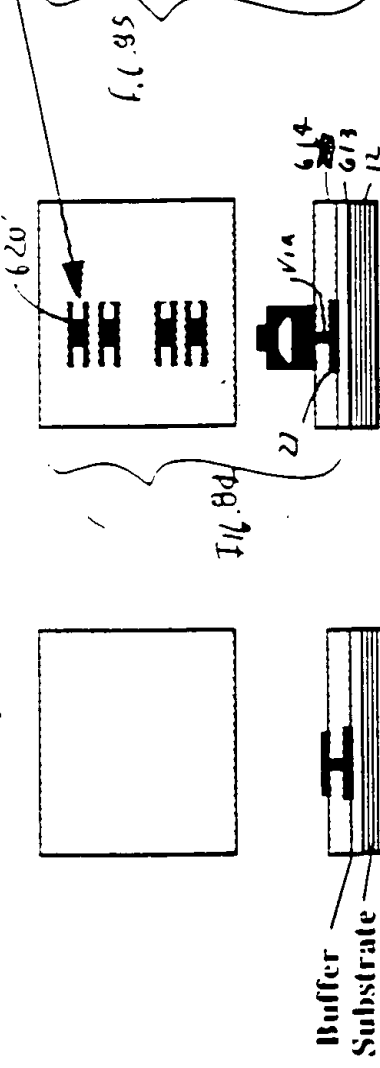


FIG. 131

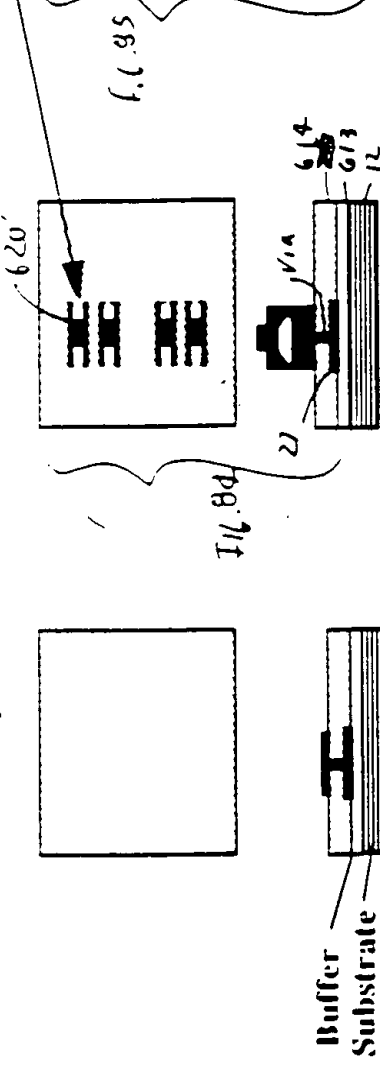


FIG. 132

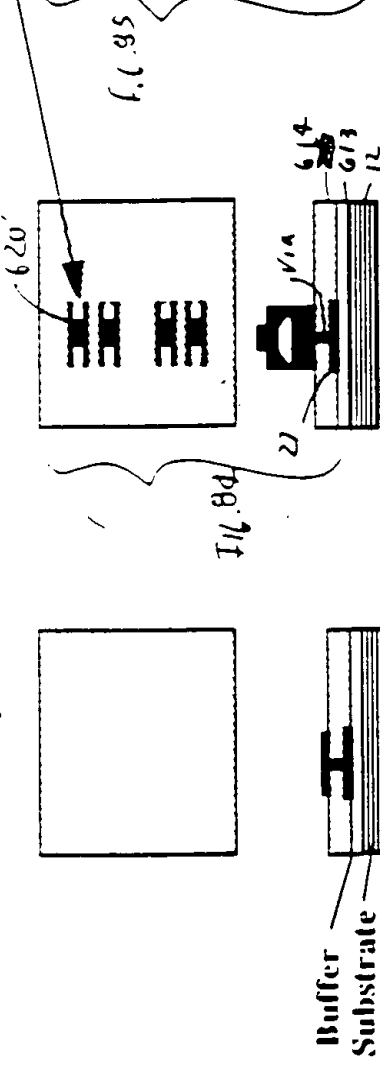


FIG. 133

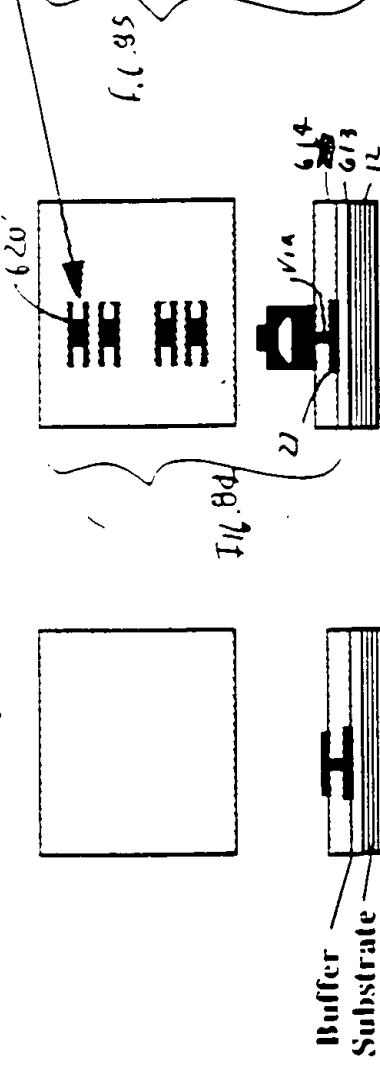


FIG. 134

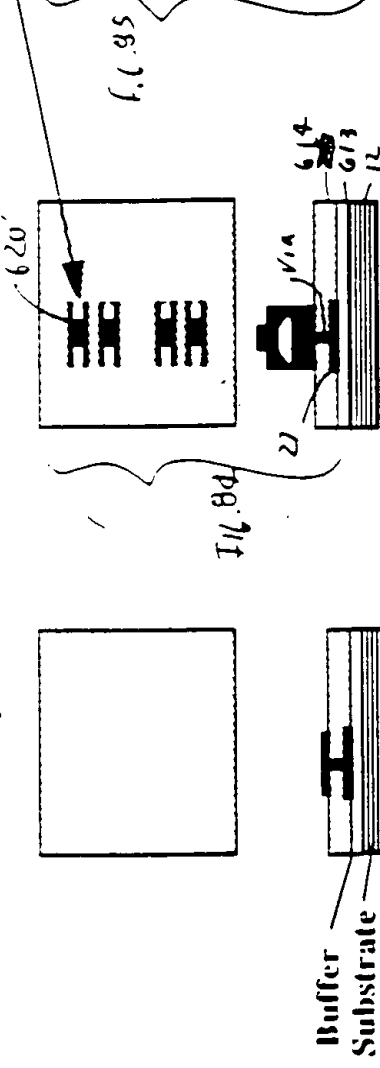


FIG. 135

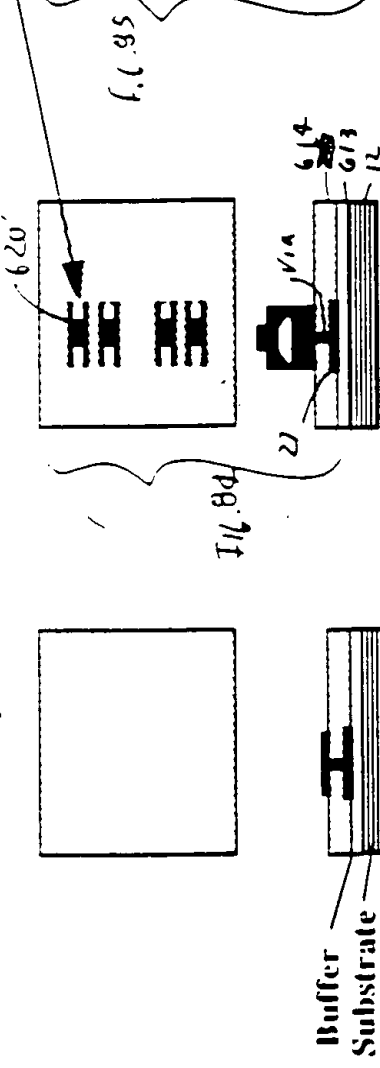


FIG. 136

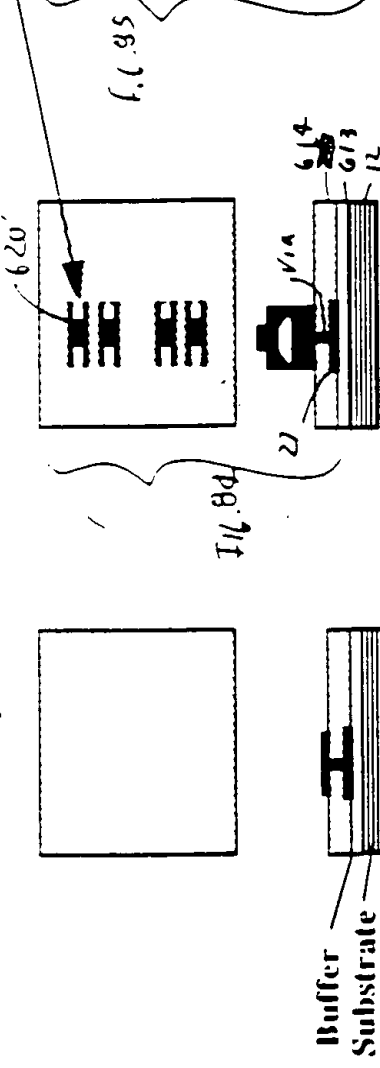


FIG. 137

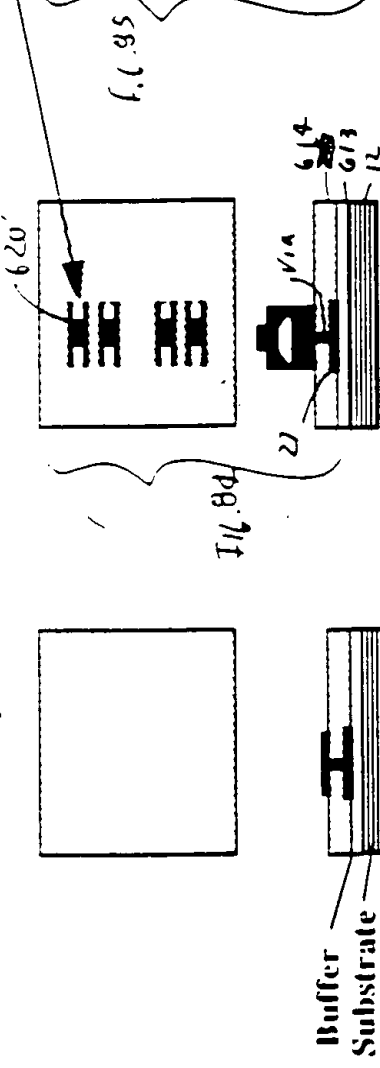


FIG. 138

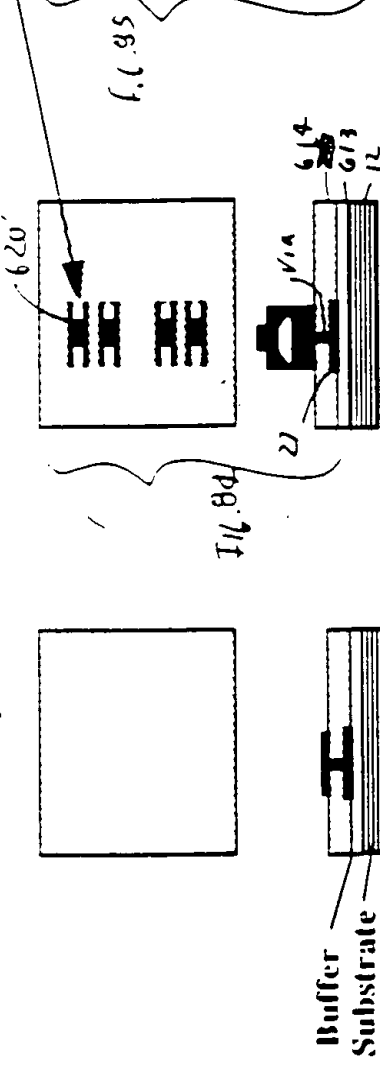


FIG. 139

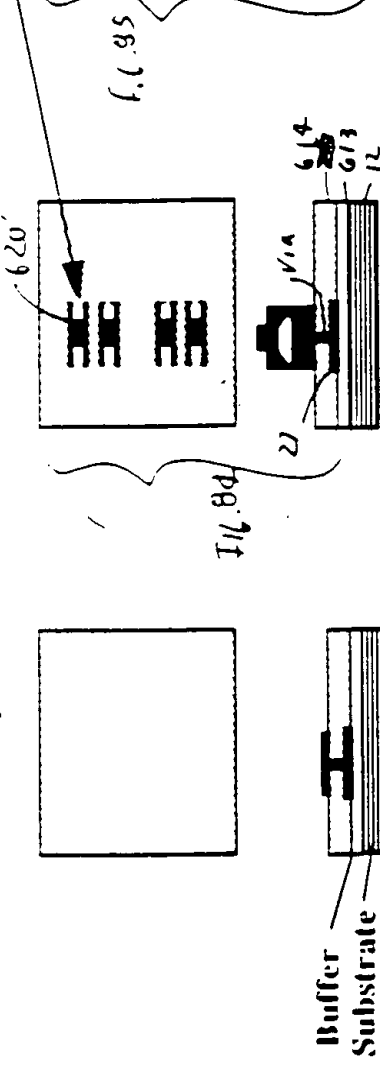


FIG. 140

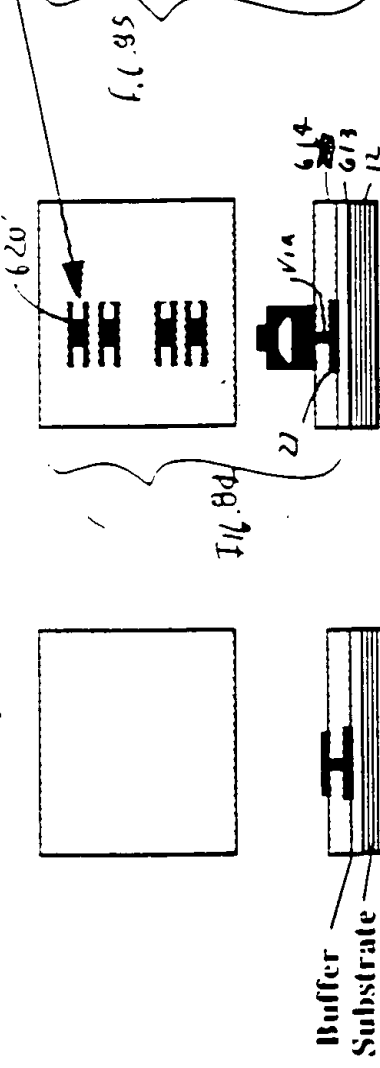


FIG. 141

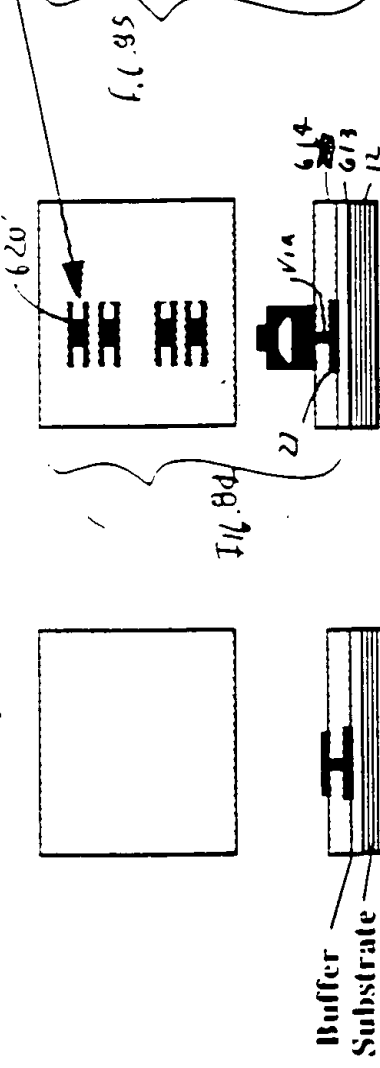


FIG. 142

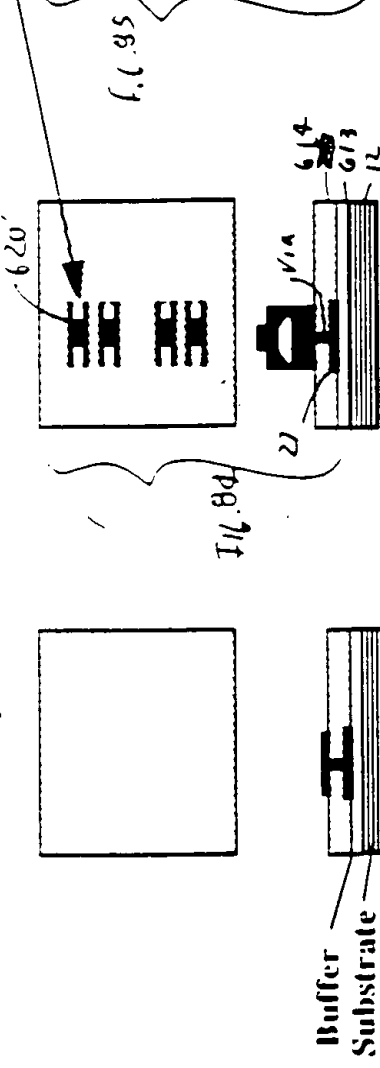


FIG. 143

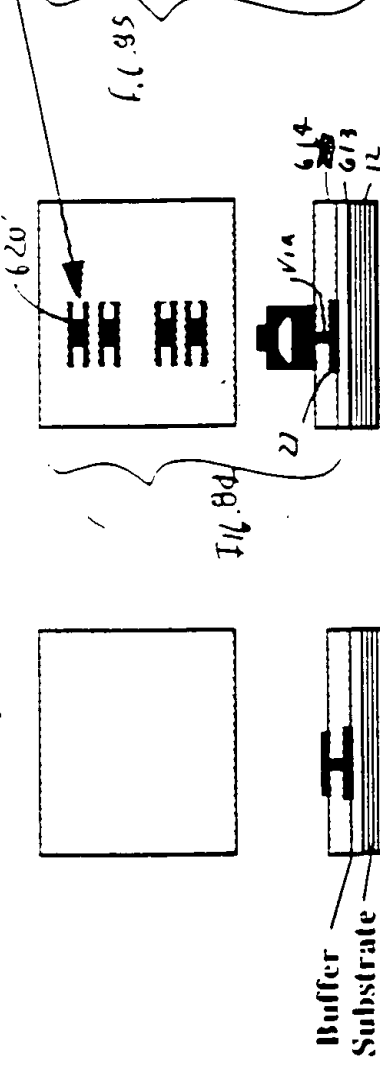


FIG. 144

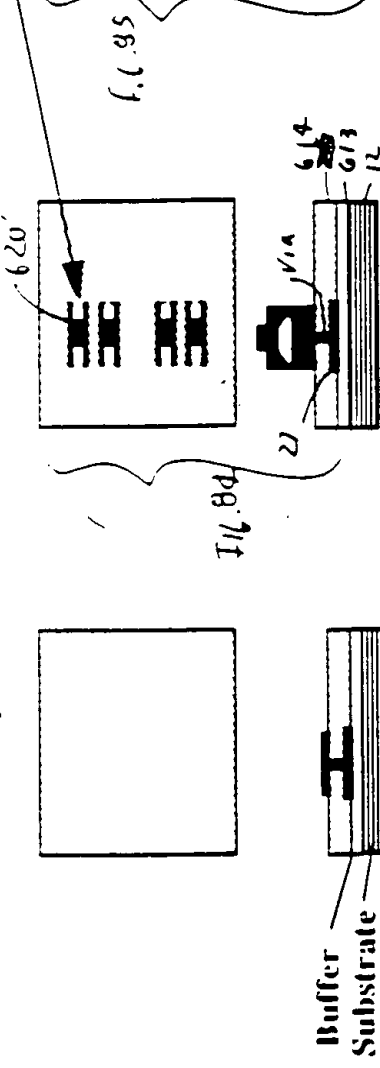


FIG. 145

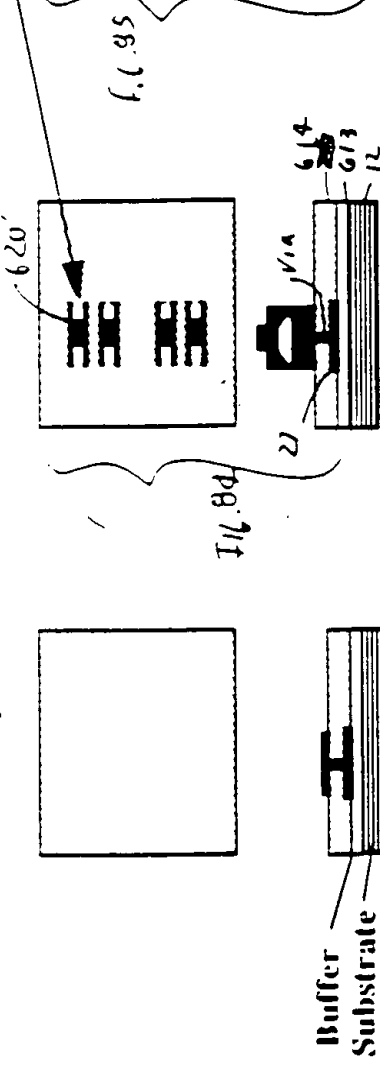


FIG. 146

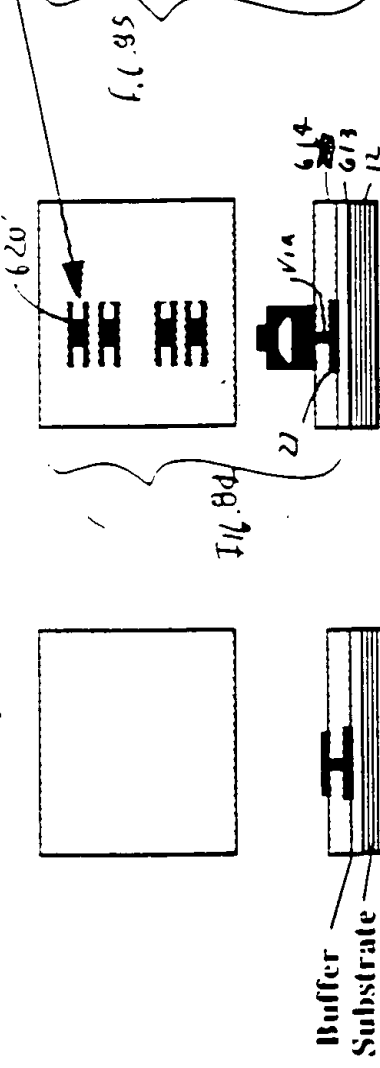


FIG. 147

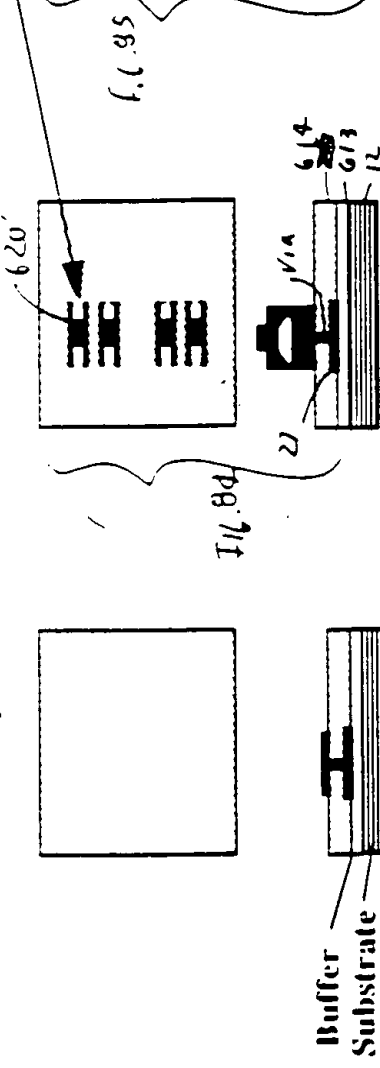


FIG. 148

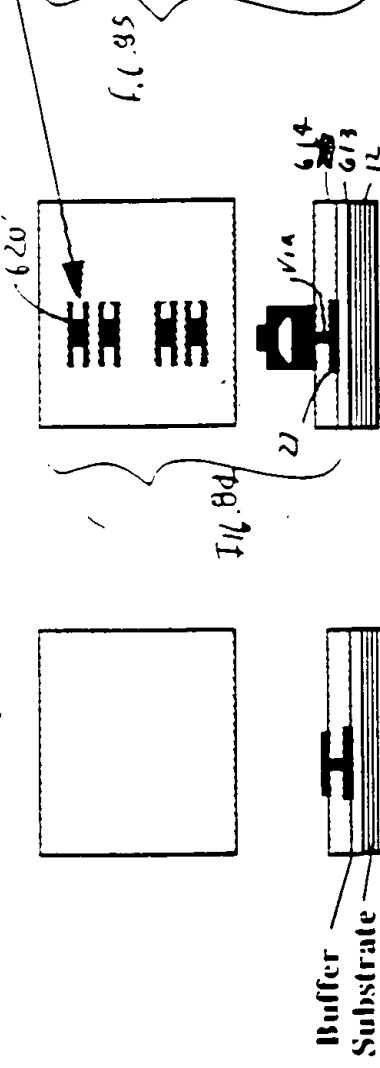


FIG. 149

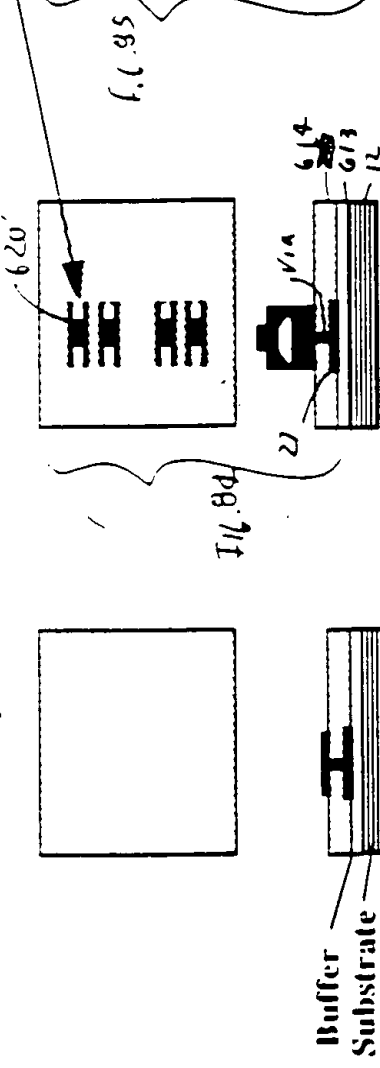


FIG. 150

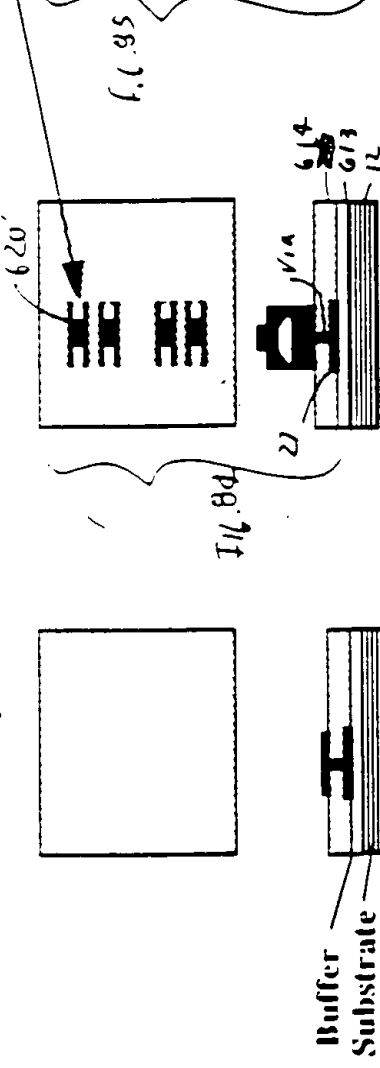


FIG. 151

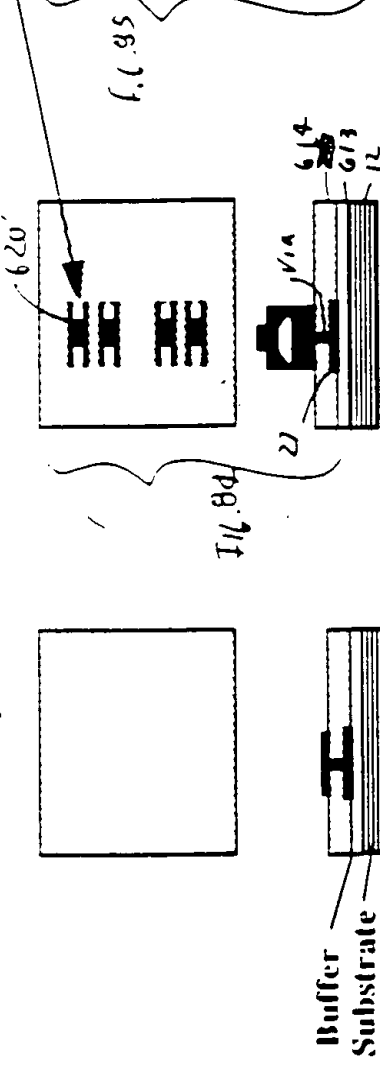


FIG. 152

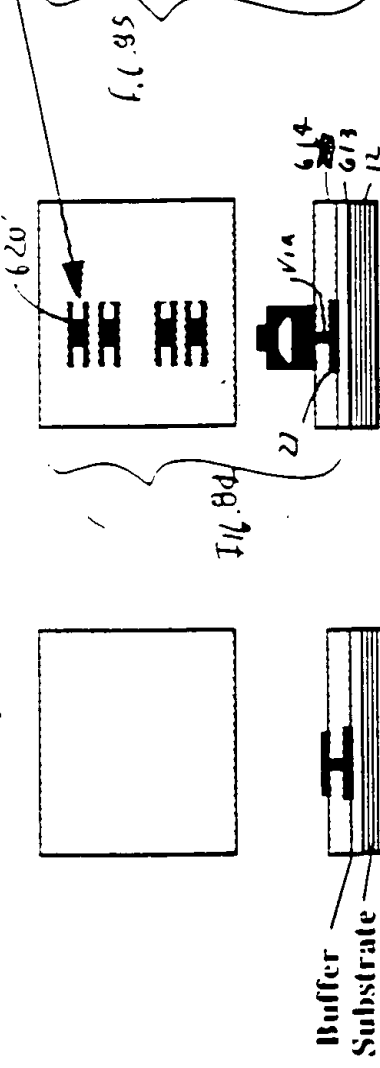


FIG. 153

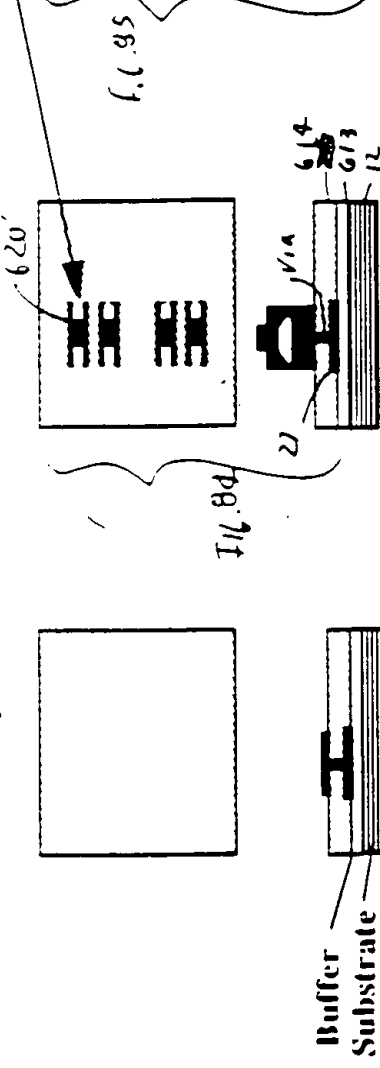


FIG. 154

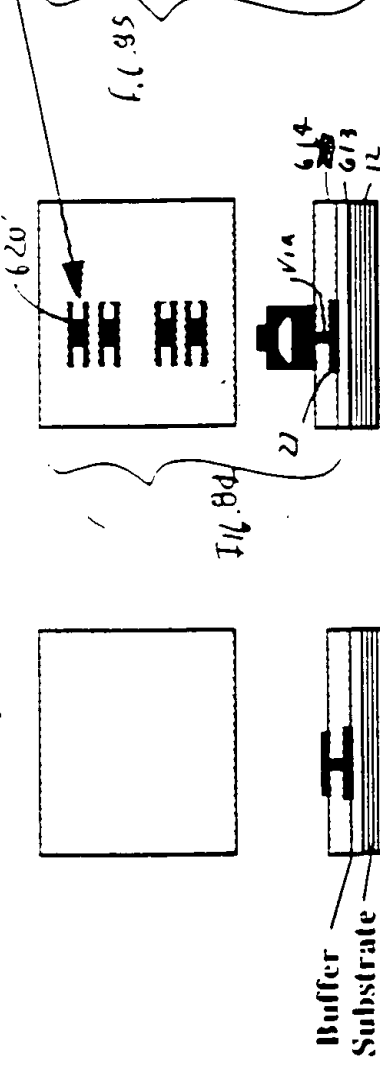


FIG. 155

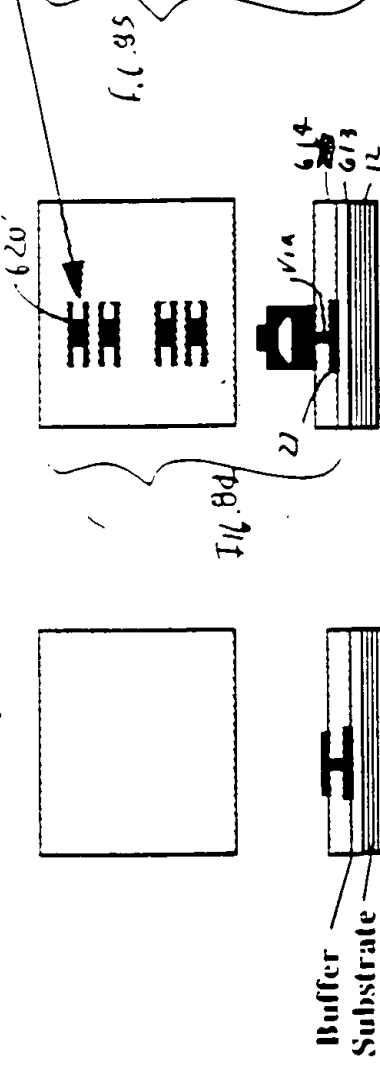


FIG. 156

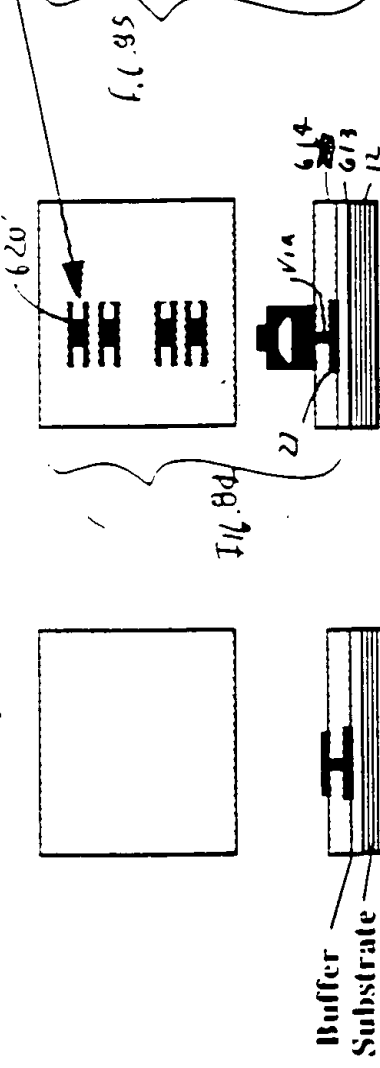


FIG. 157

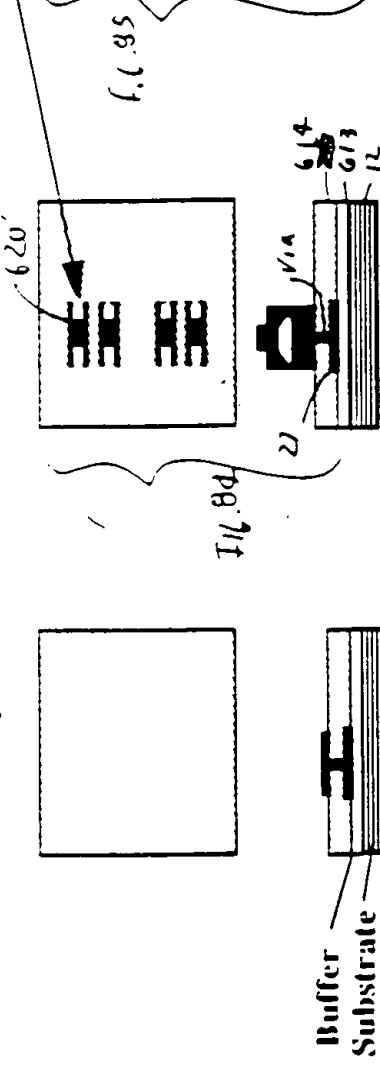


FIG. 158

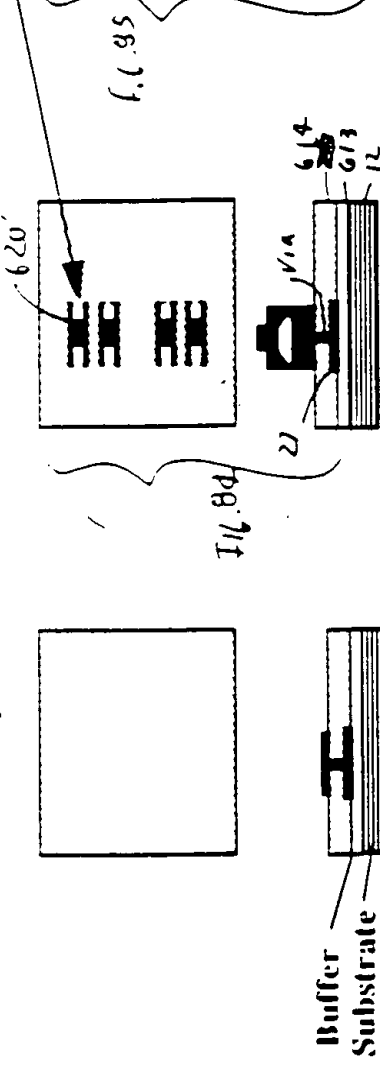


FIG. 159

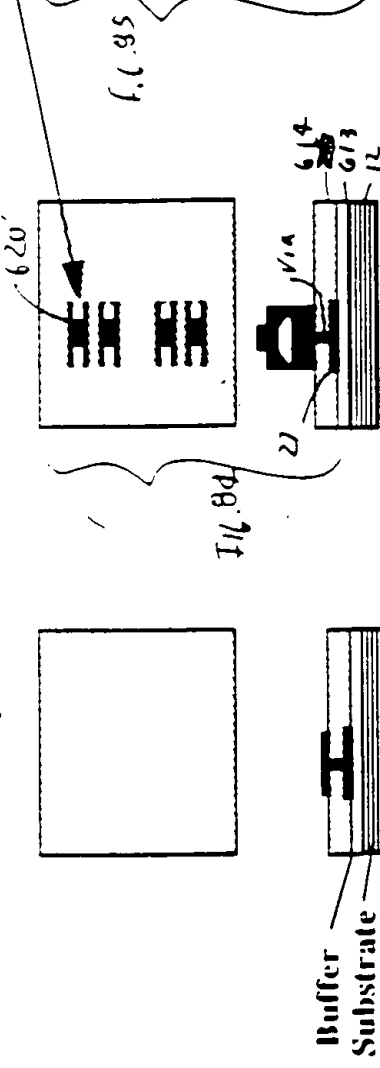


FIG. 160

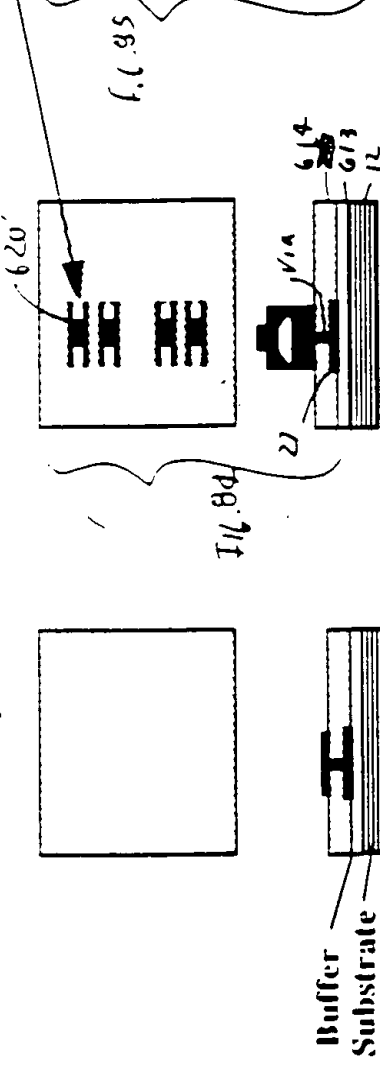


FIG. 161

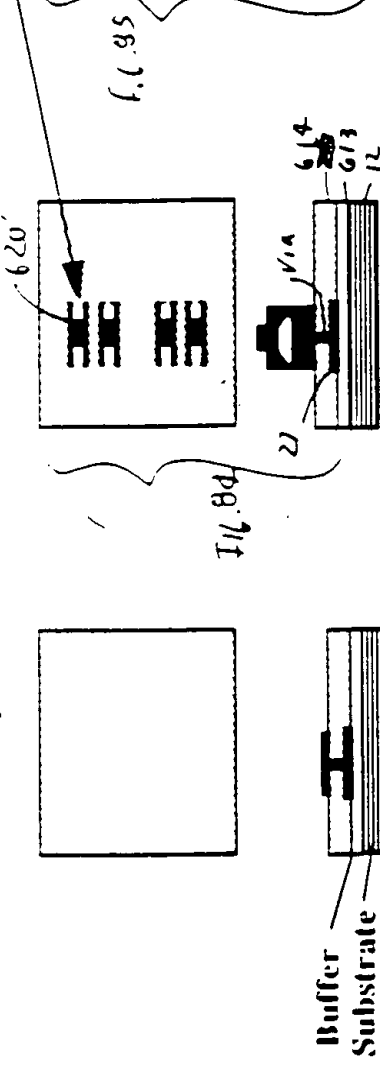


FIG. 162

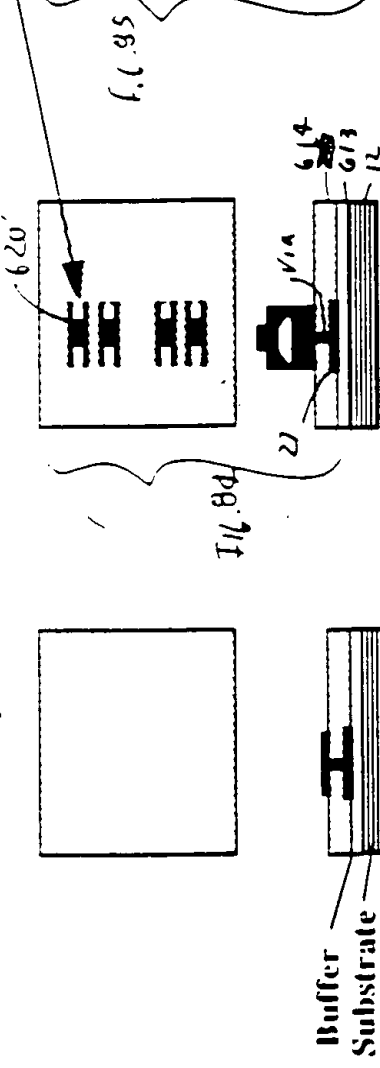


FIG. 163

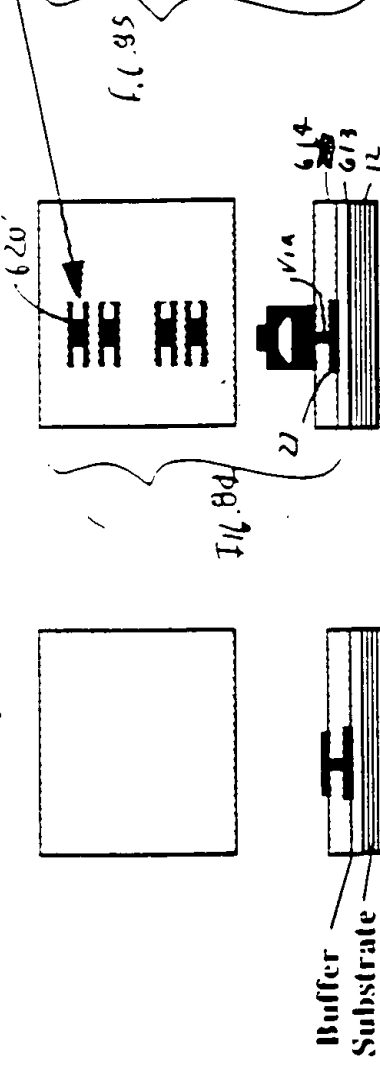


FIG. 164

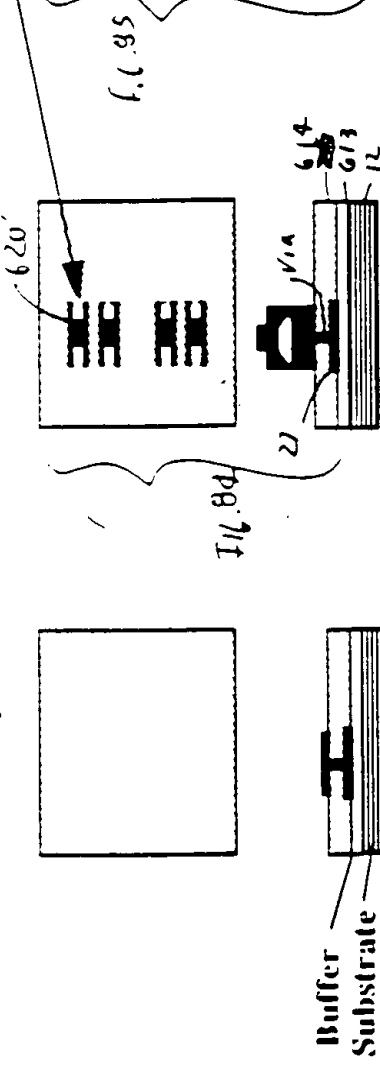


FIG. 165

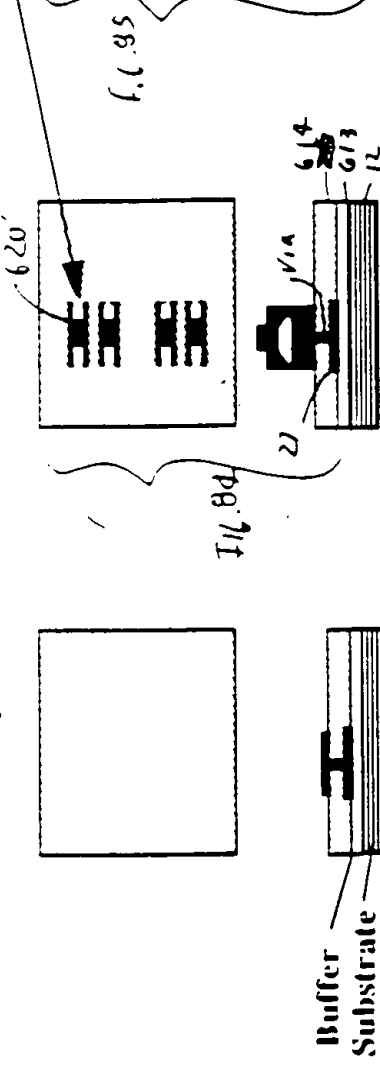


FIG. 166

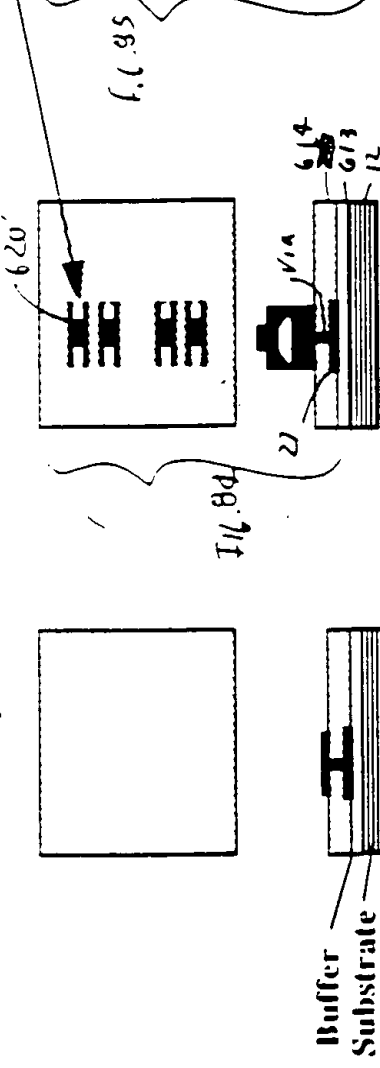


FIG. 167

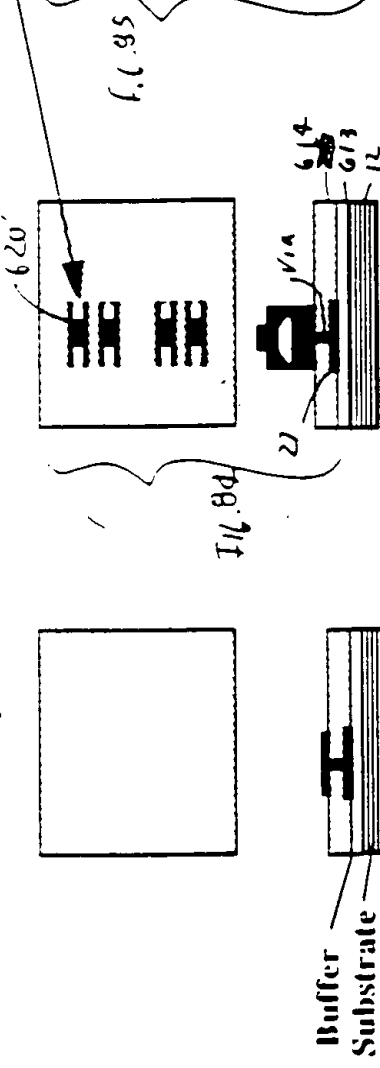


FIG. 168

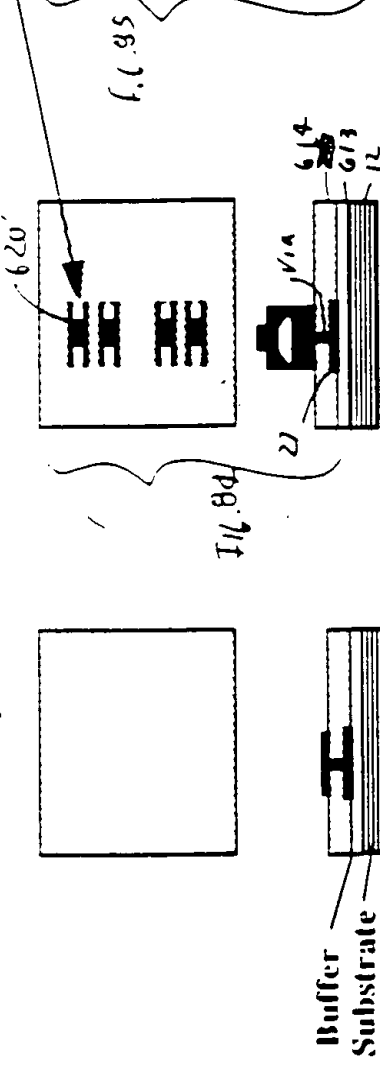


FIG. 169

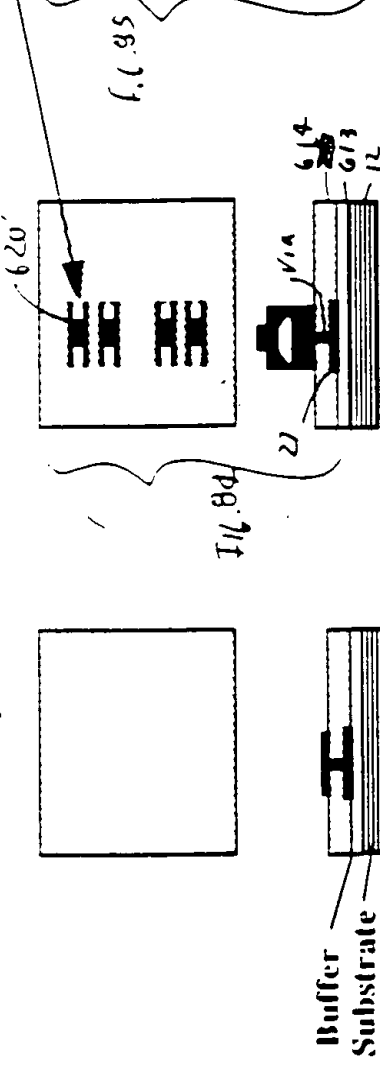


FIG. 170

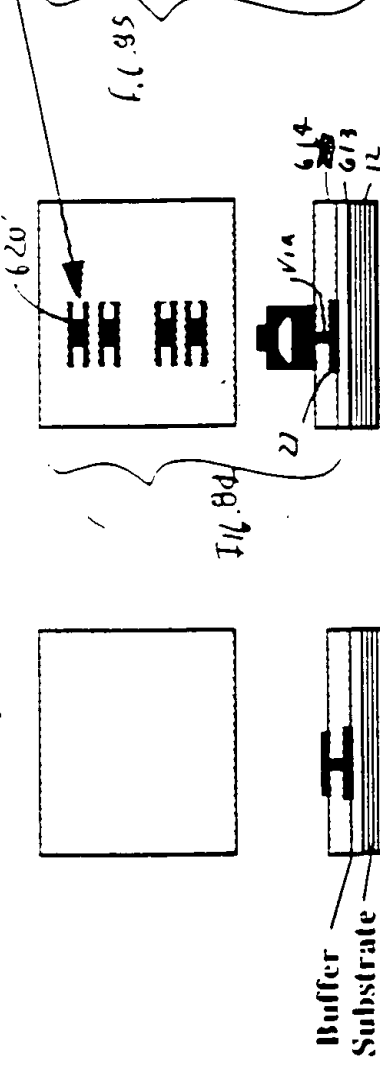


FIG. 171

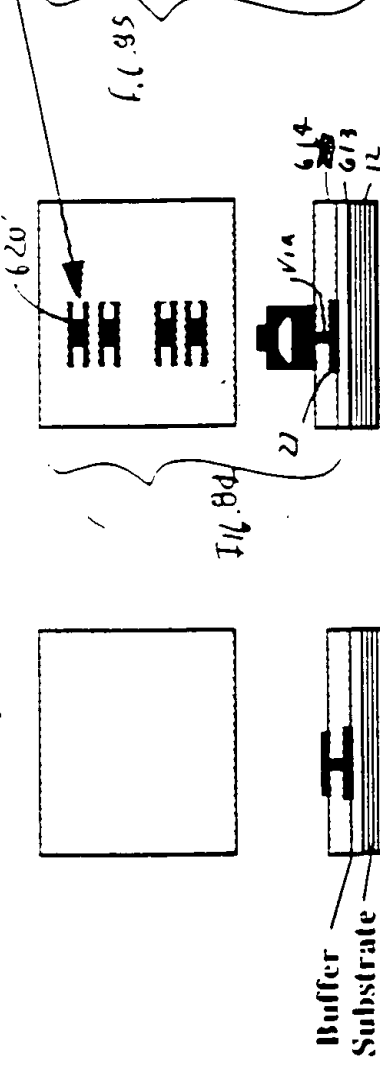


FIG. 172

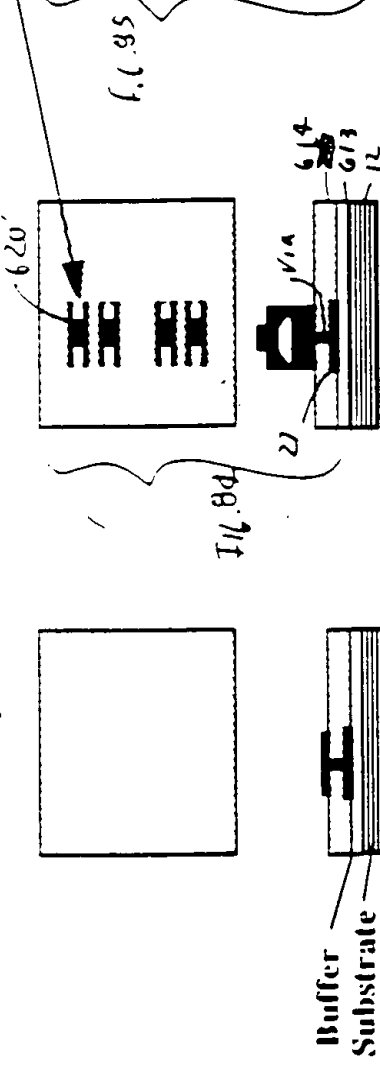


FIG. 173

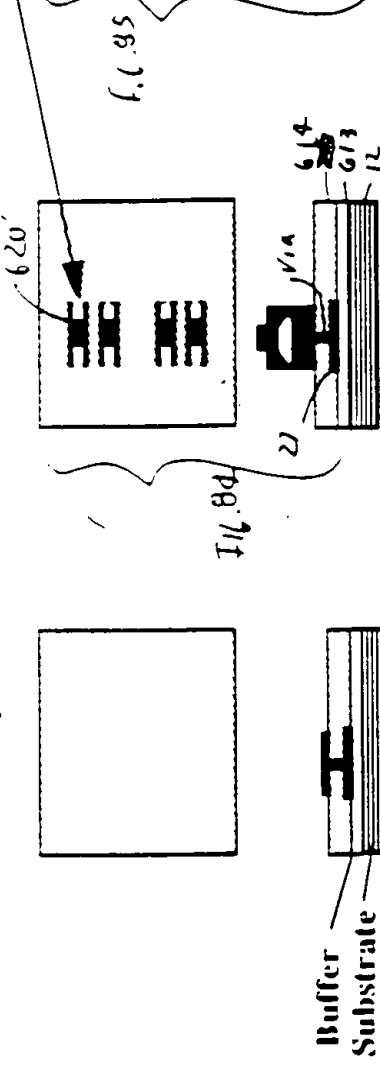


FIG. 174

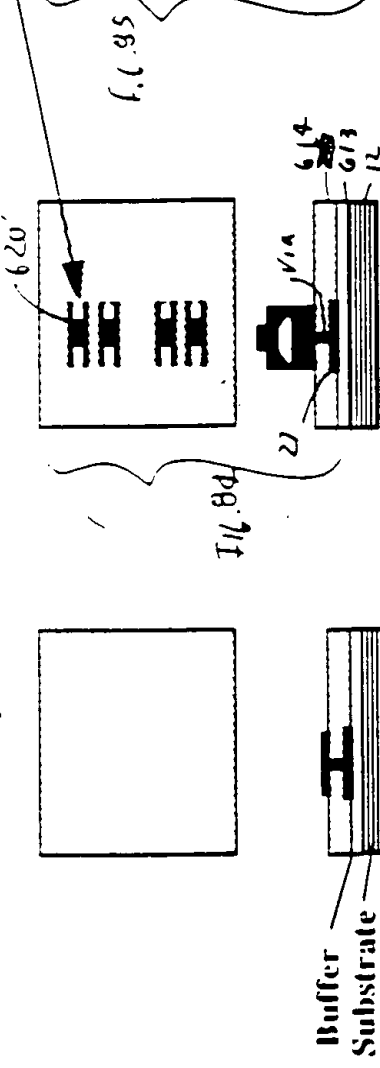


FIG. 175

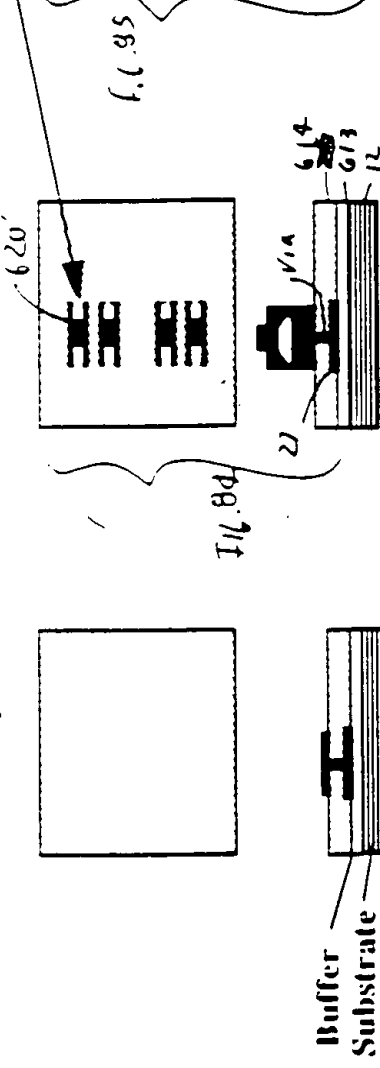


FIG. 176

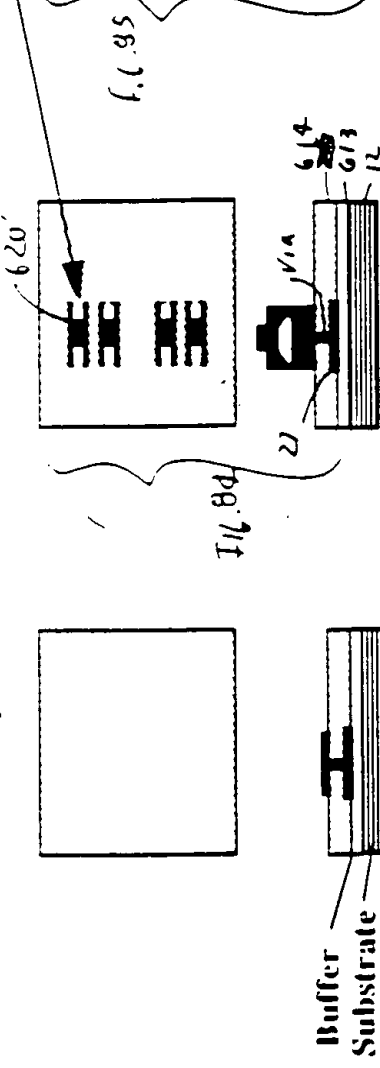


FIG. 177

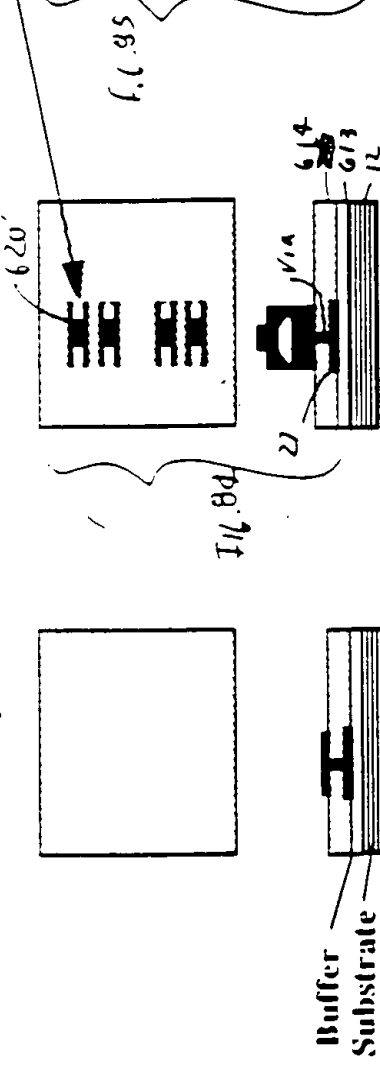


FIG. 178

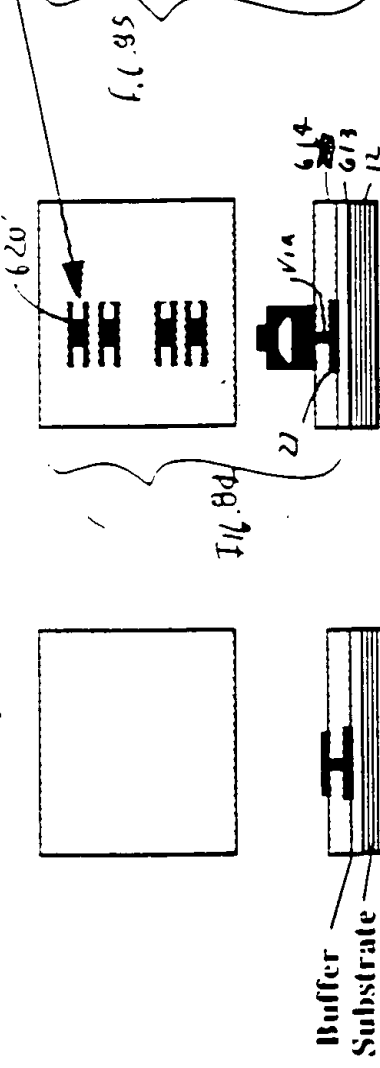


FIG. 179

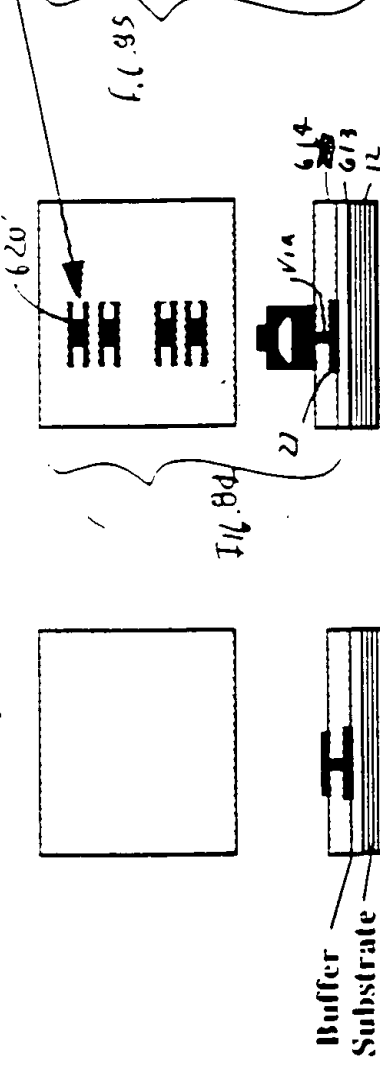


FIG. 180

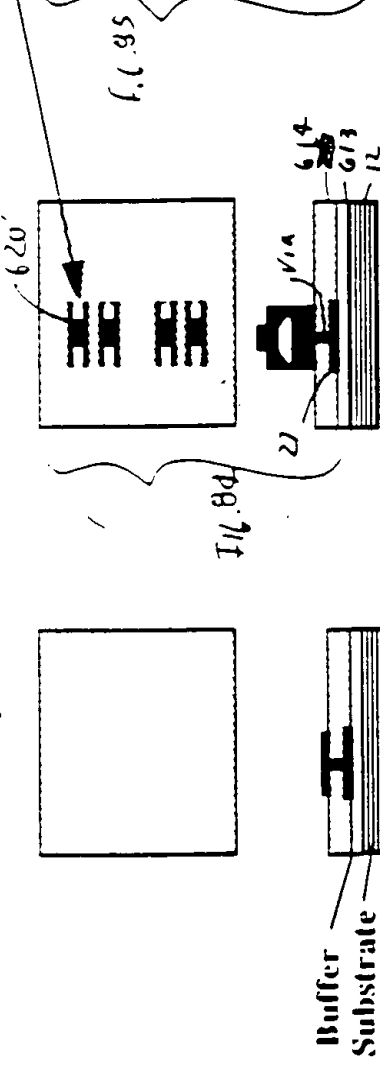


FIG. 181

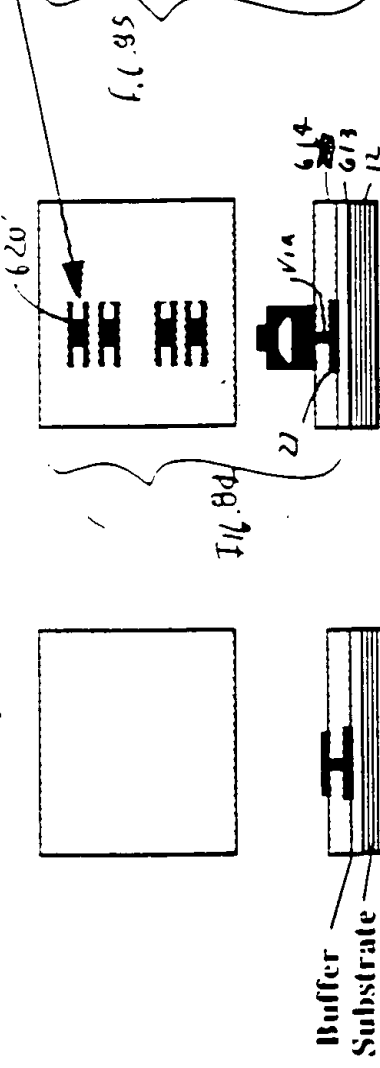


FIG. 182

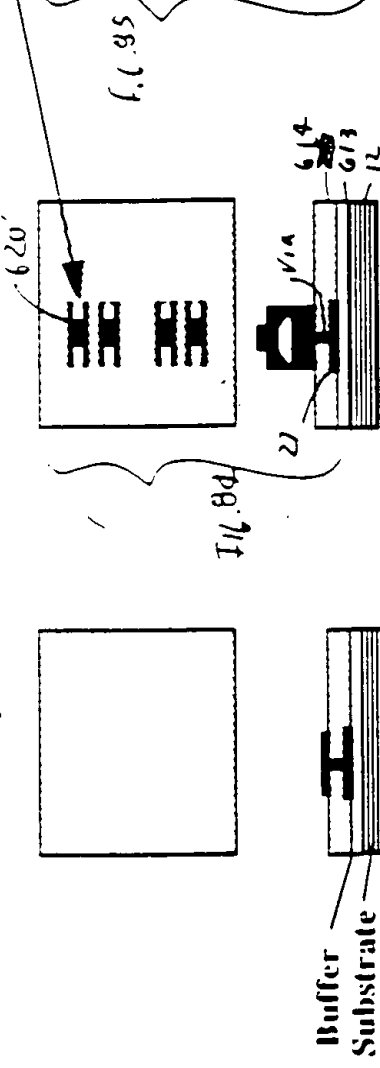


FIG. 183

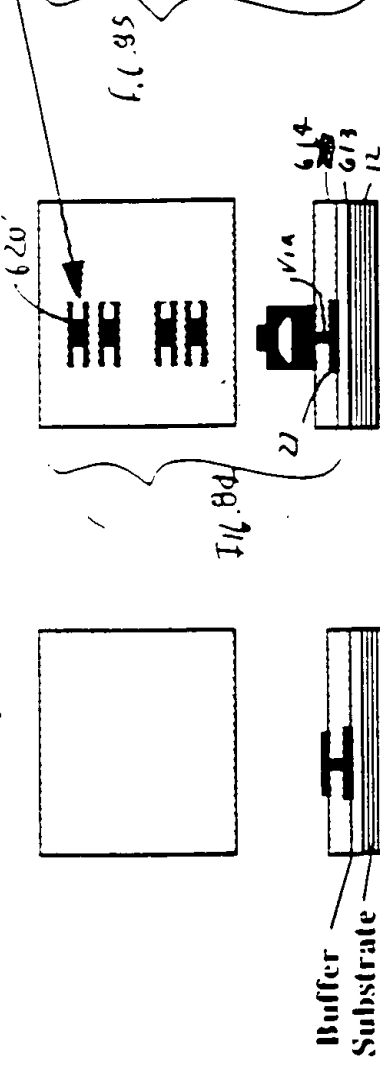
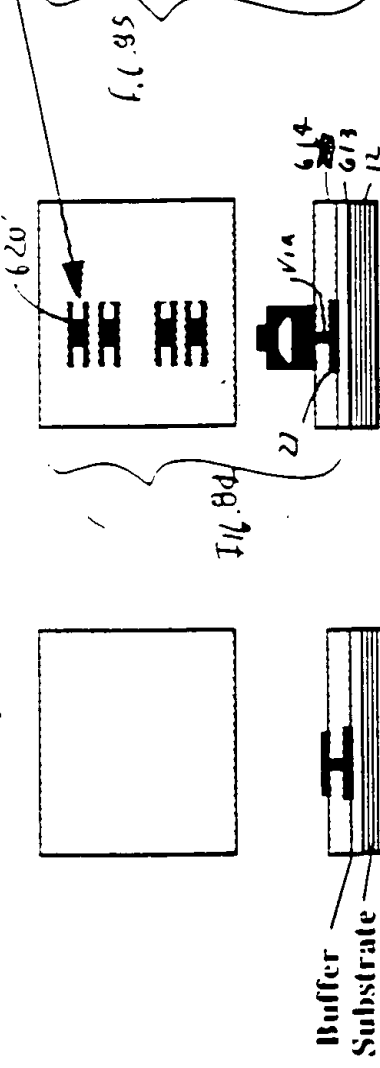
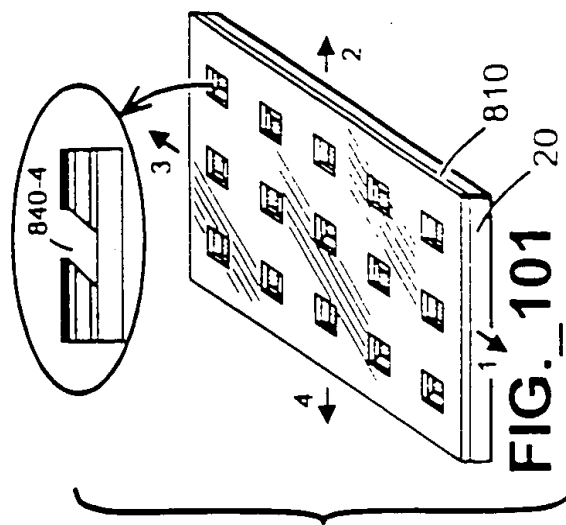
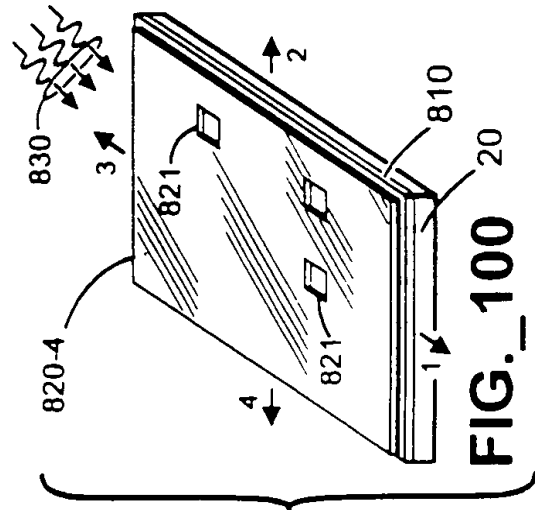
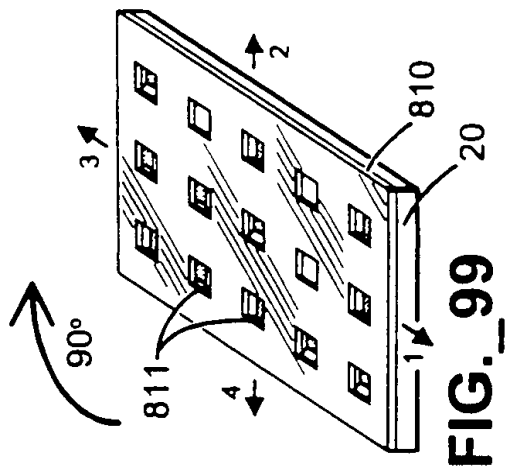
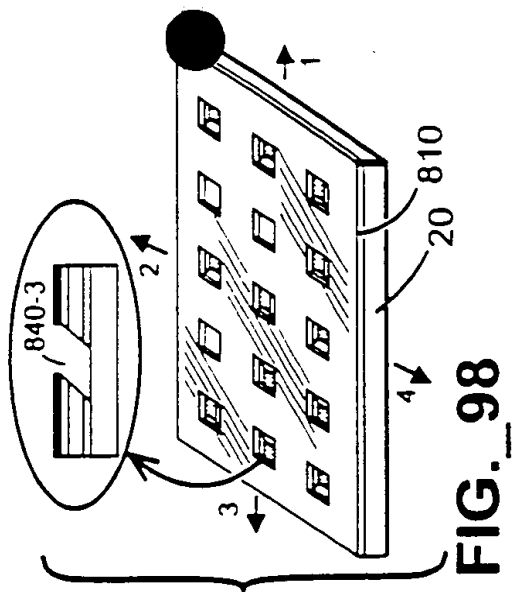
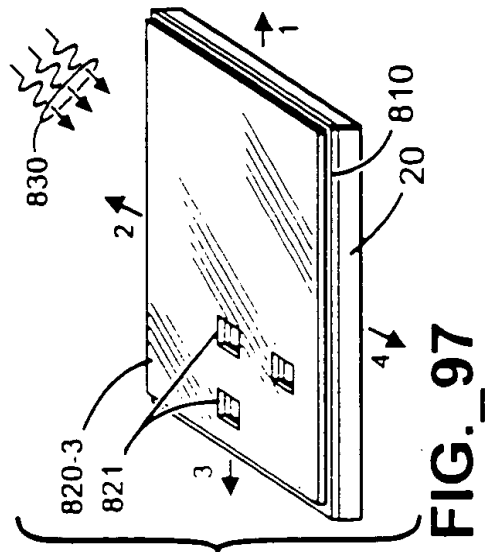
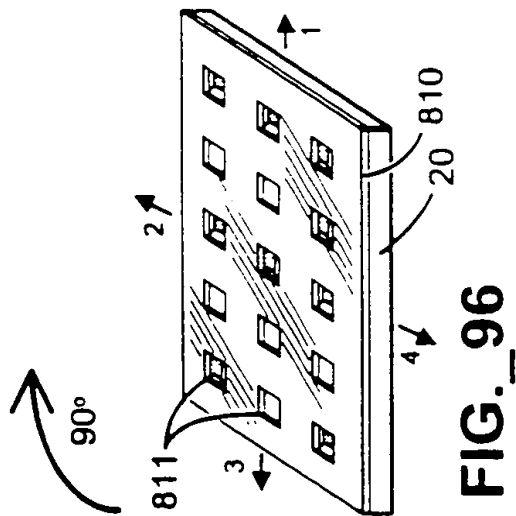


FIG. 184





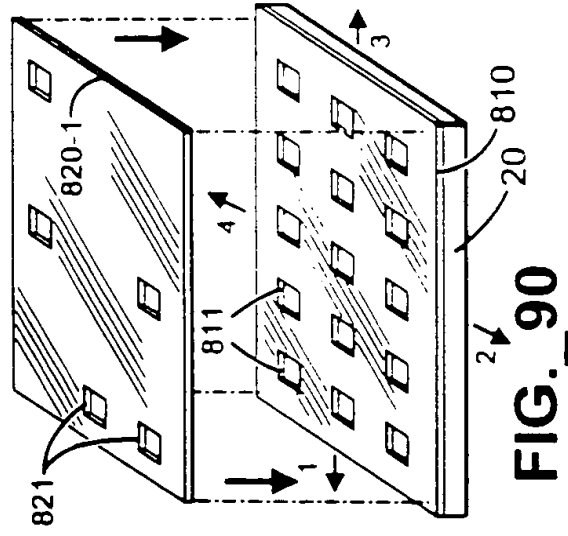


FIG. 90

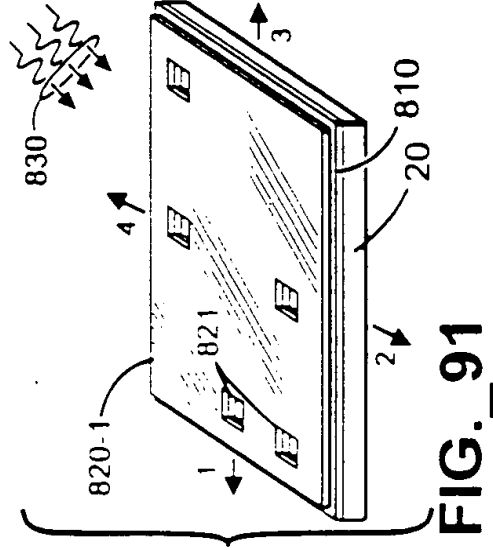


FIG. 91

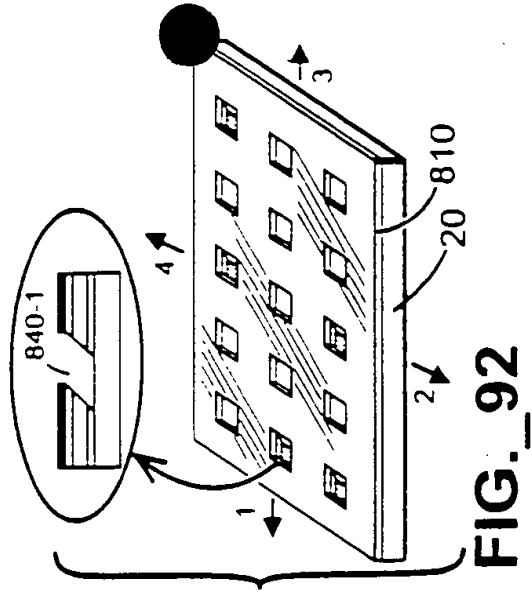


FIG. 92

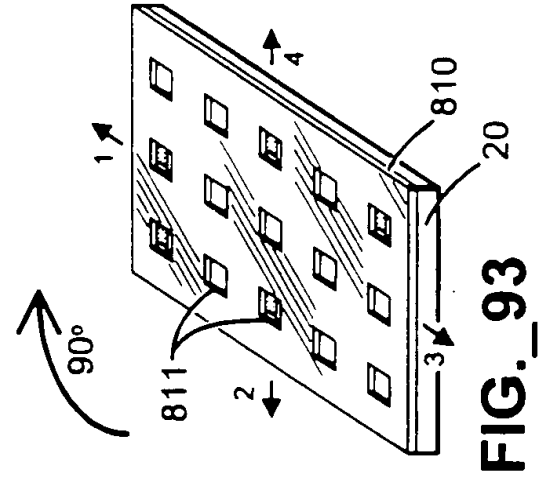


FIG. 93

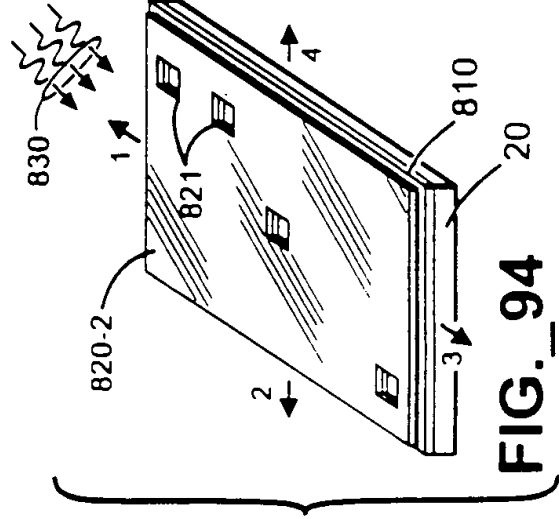


FIG. 94

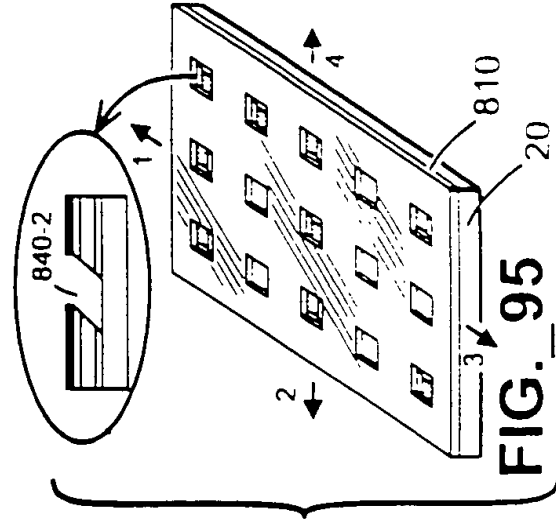
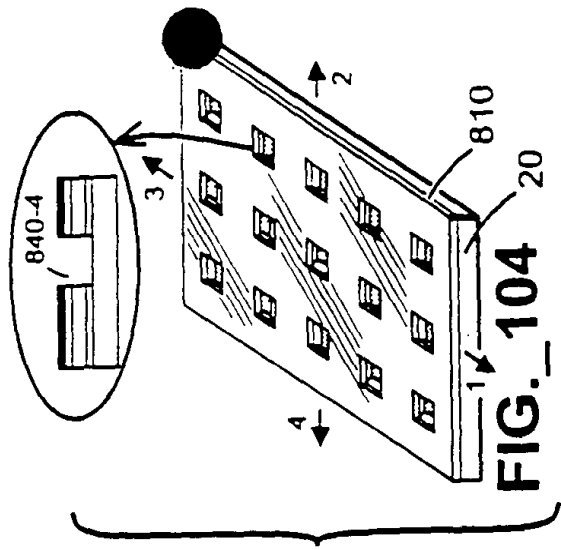
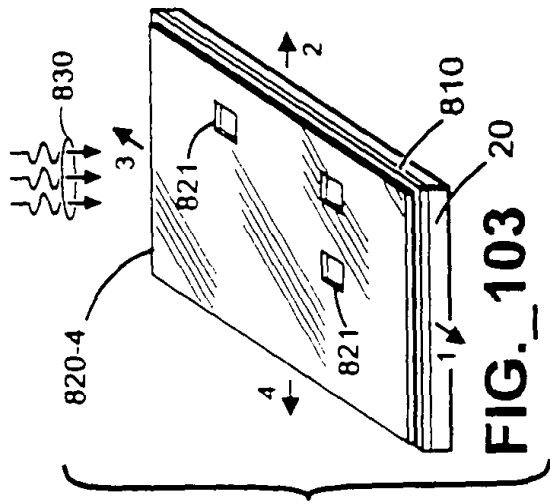
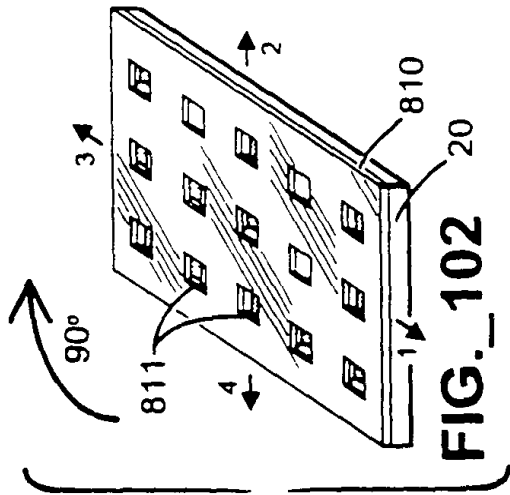


FIG. 95



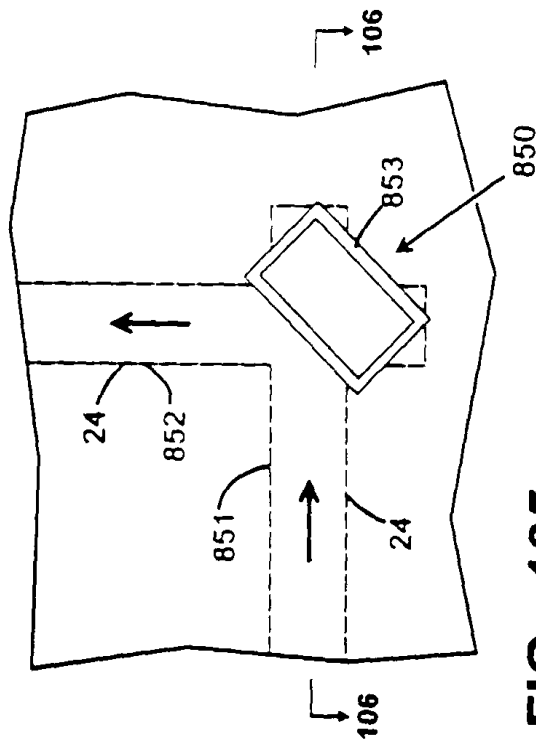


FIG. 105

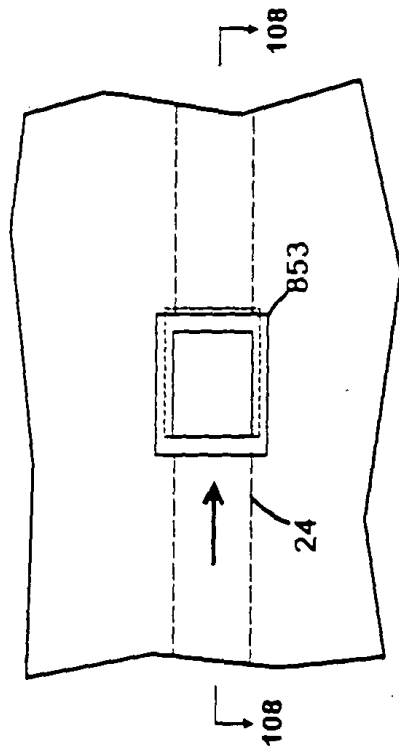


FIG. 107

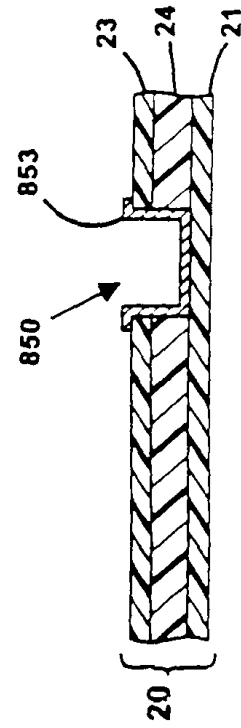


FIG. 106

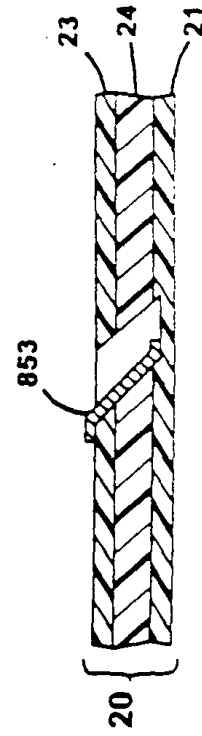
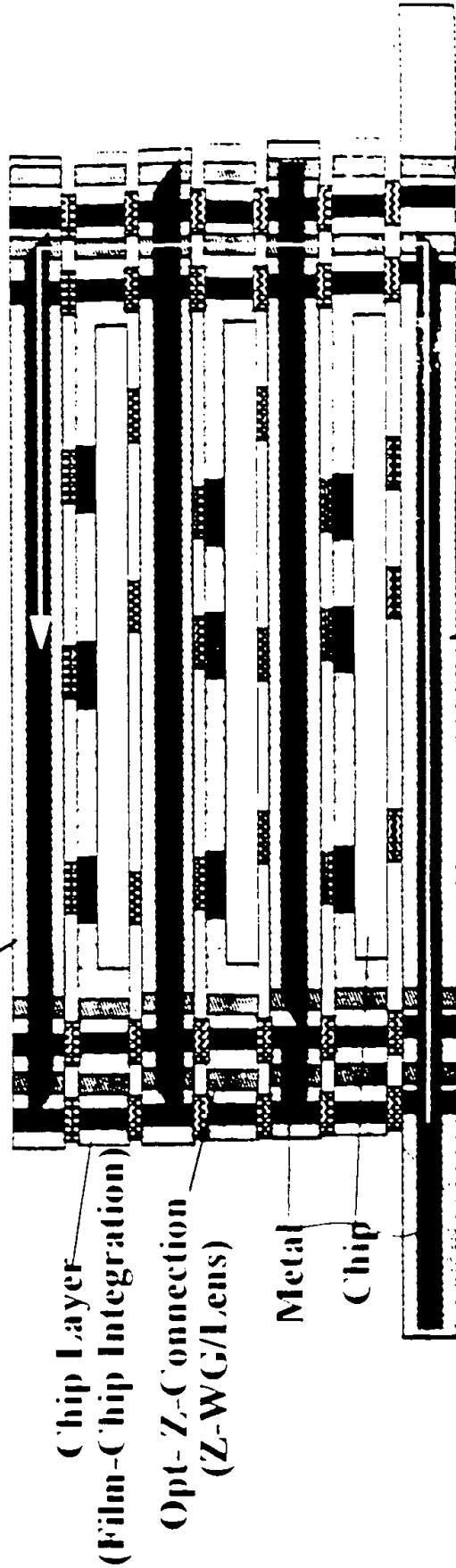


FIG. 108

GS CX/CXX OE Solution --- OE-3D-Stack

OE-film-DH' (V) or (M)



OE-film-DH'

A-A'

FIG. 109

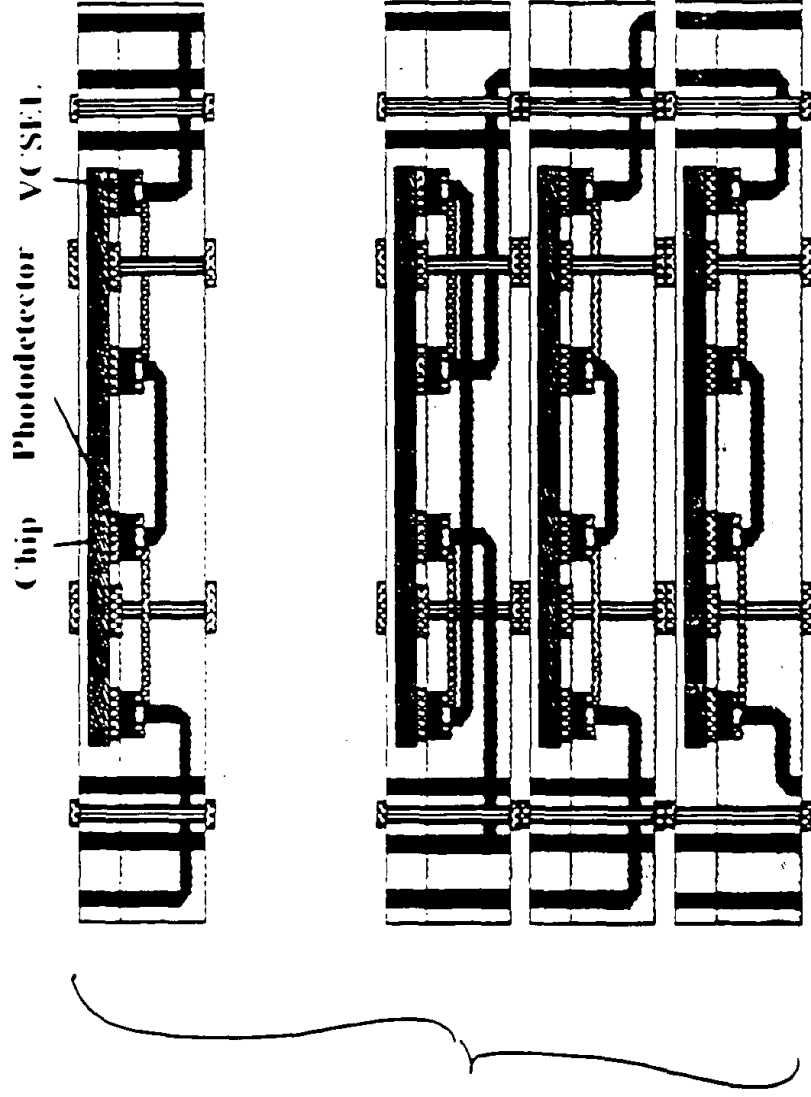


Fig. 110

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

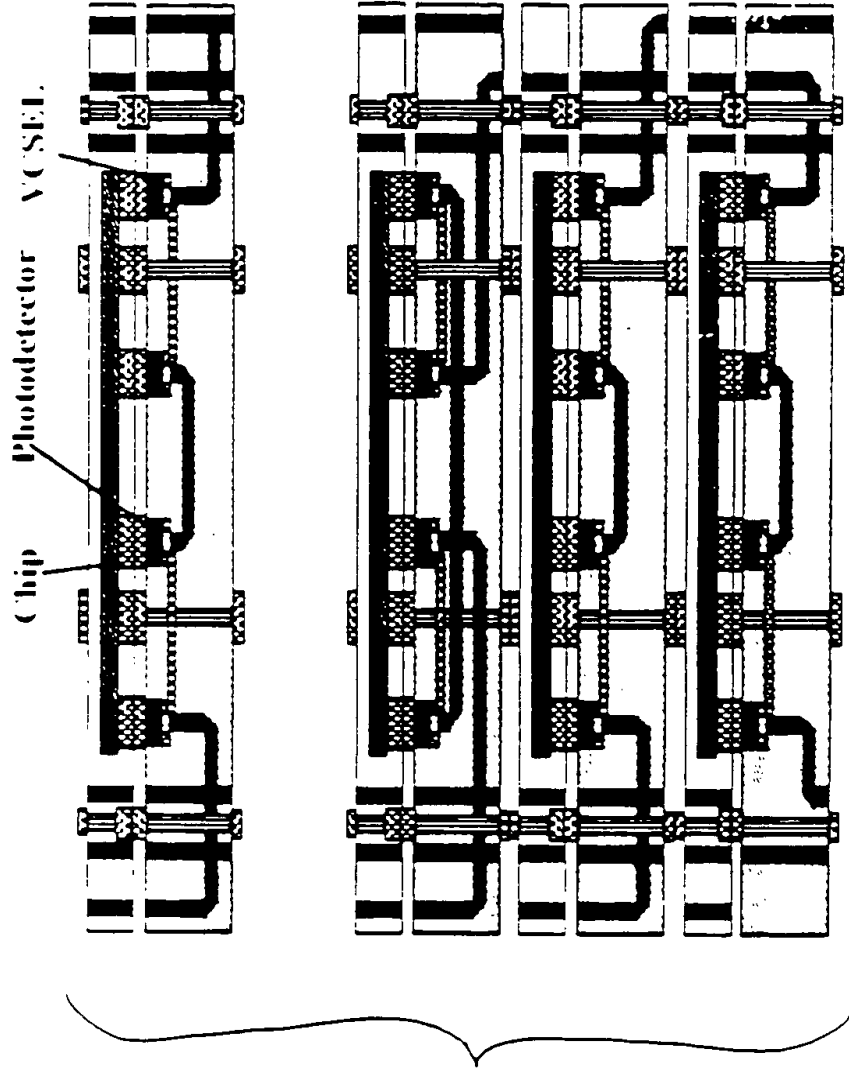


Fig. 110

A24

(2/23/99) AA2 Detail picture Example for 3D-stack

(New version of the AA2 of 2/5/99)

FUJITSU Computer Packaging Technologies, Inc. **FCPT**
Film/Z-Connection Application to OE-Substrate

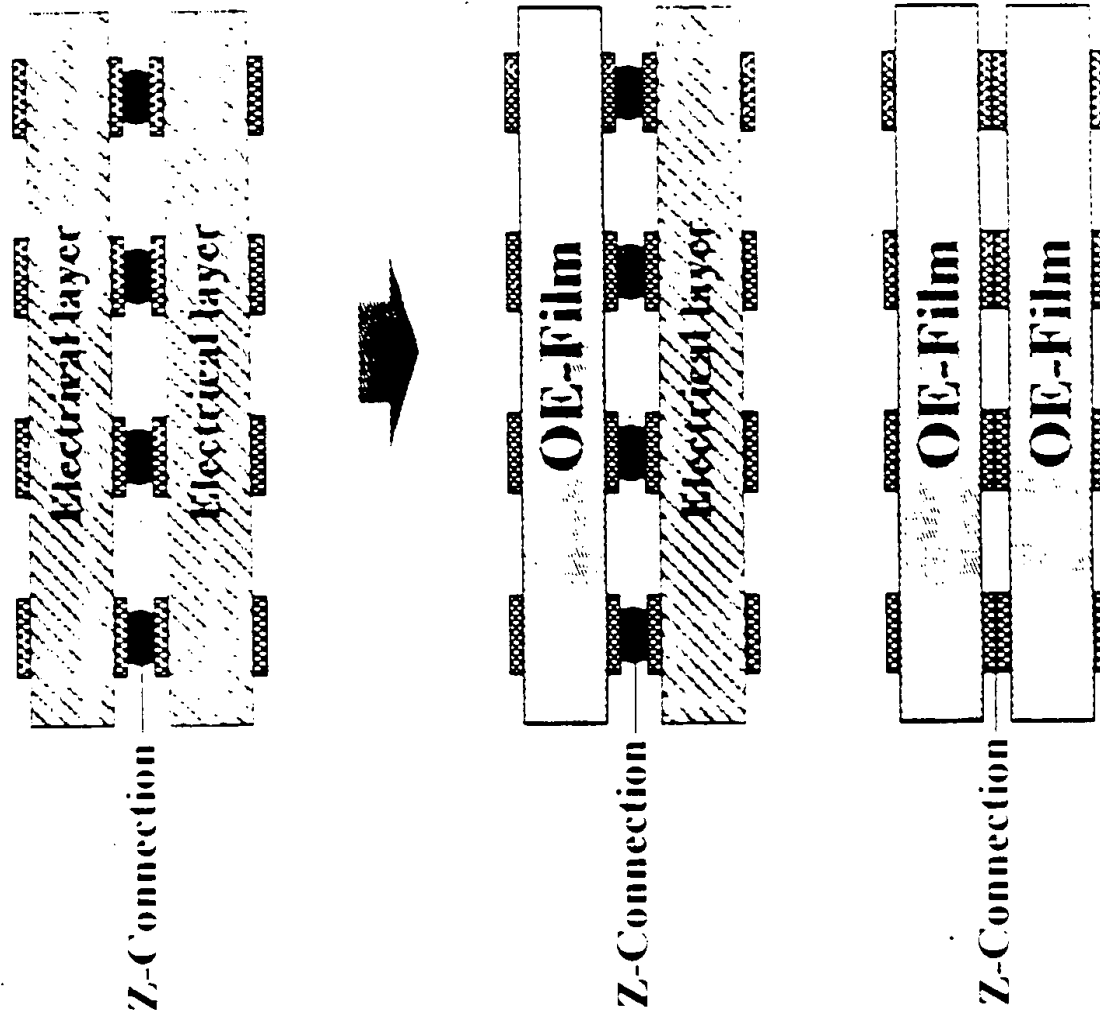
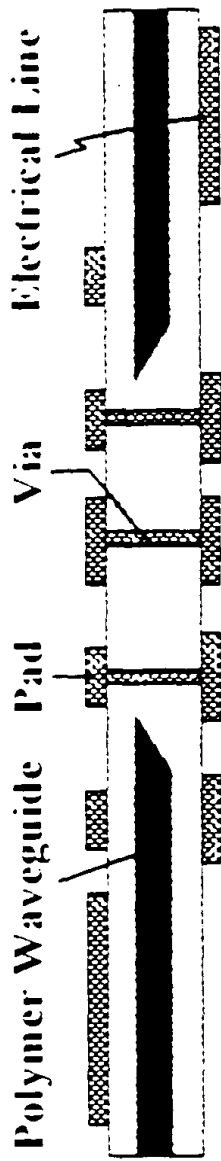


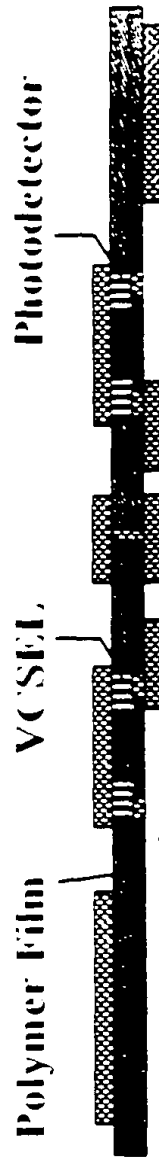
Fig. 1/2

OE-Films



OE-film-W

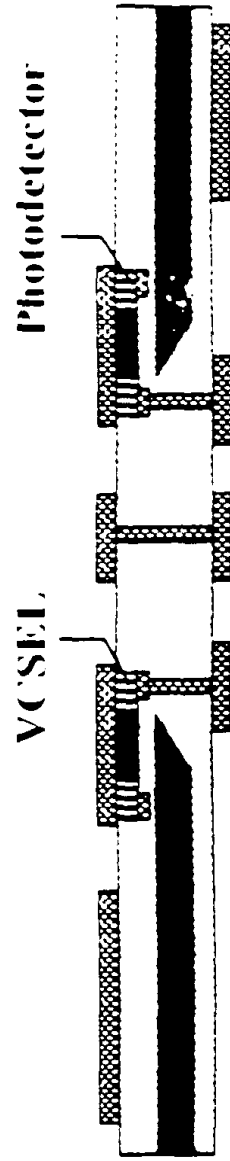
FIG. 113



OE-film-D

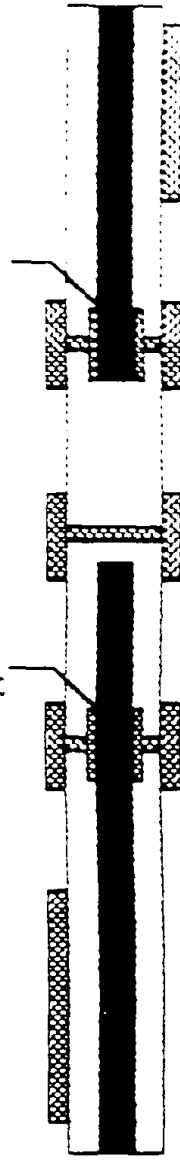
FIG. 114

A8



OE-film-DIW(V)

FIG. 115



OE-film-DIW(M)

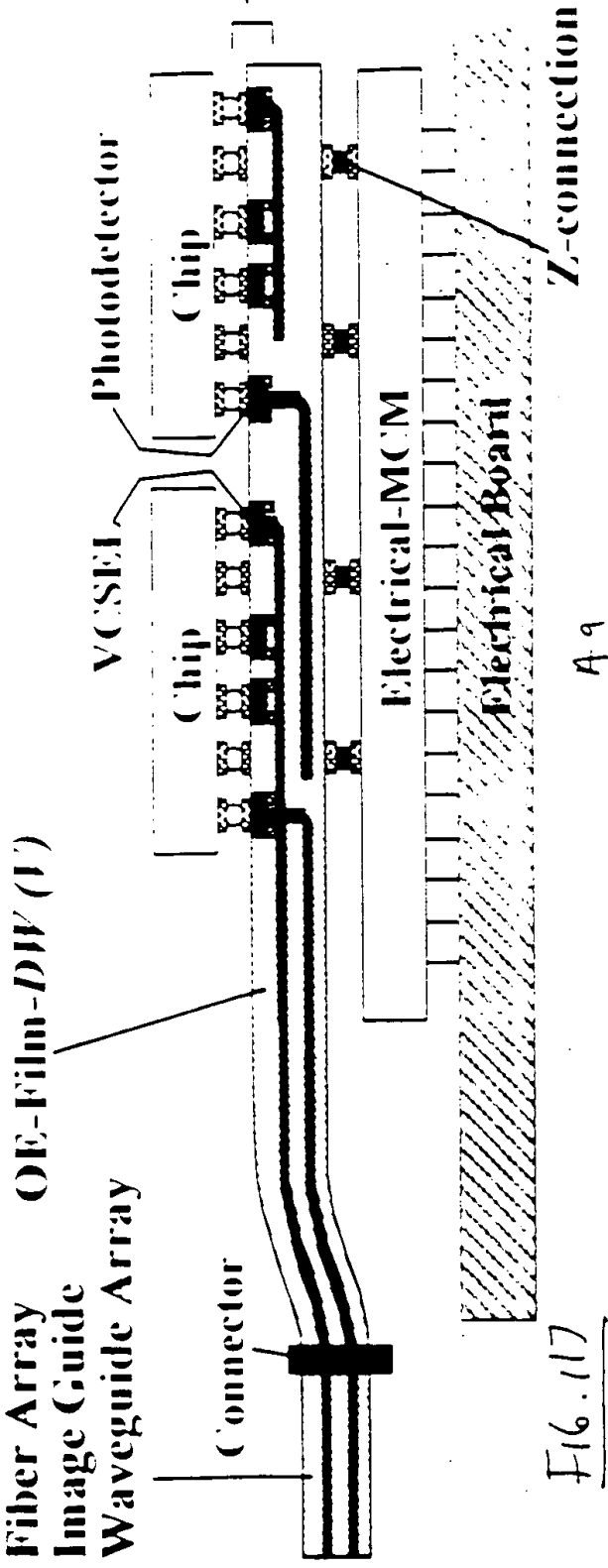
2/17/99-added 2

FIG. 116

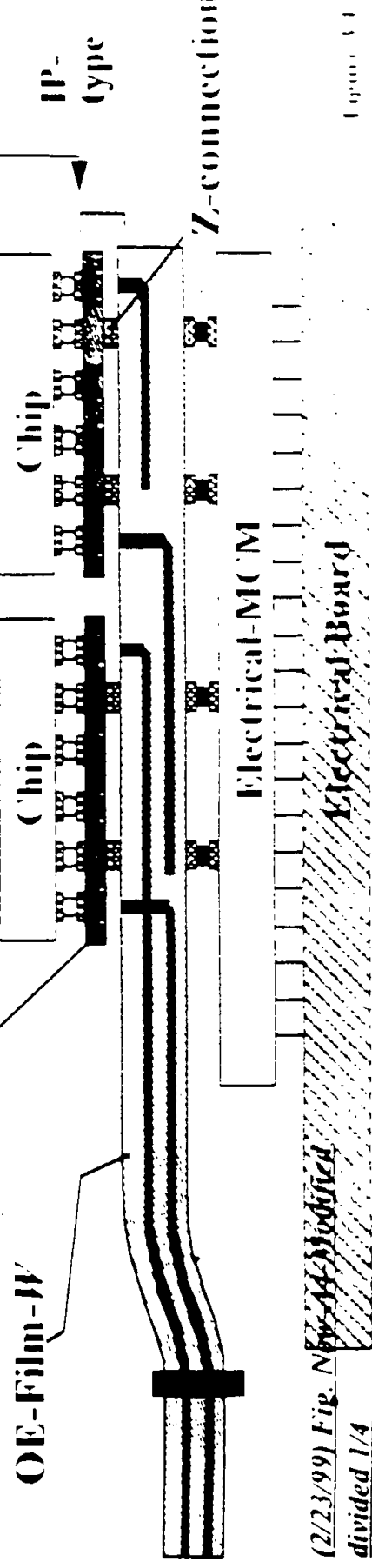
20 172

FOLM

Fiber Array
Image Guide
Waveguide Array



OE-Film-D



(2/23/99) Fig. New-14 Modified
divided 1/4

FIG. 118
A0 217/90

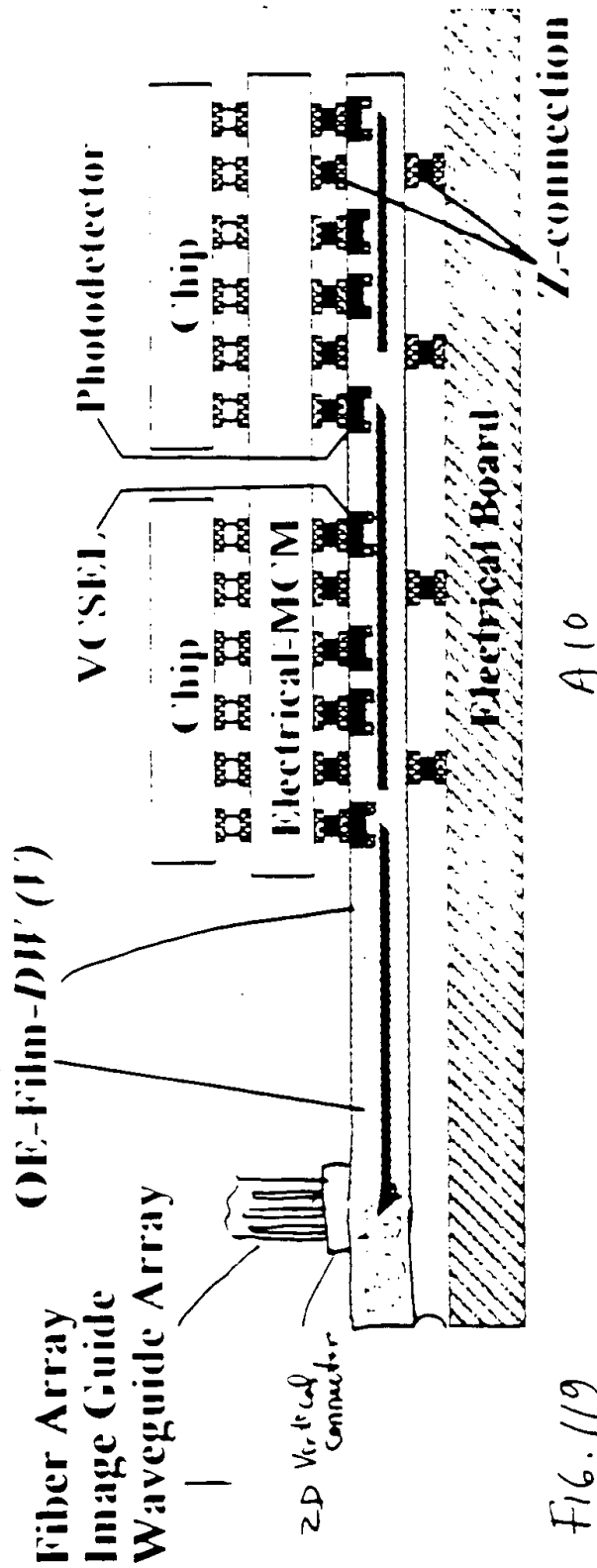
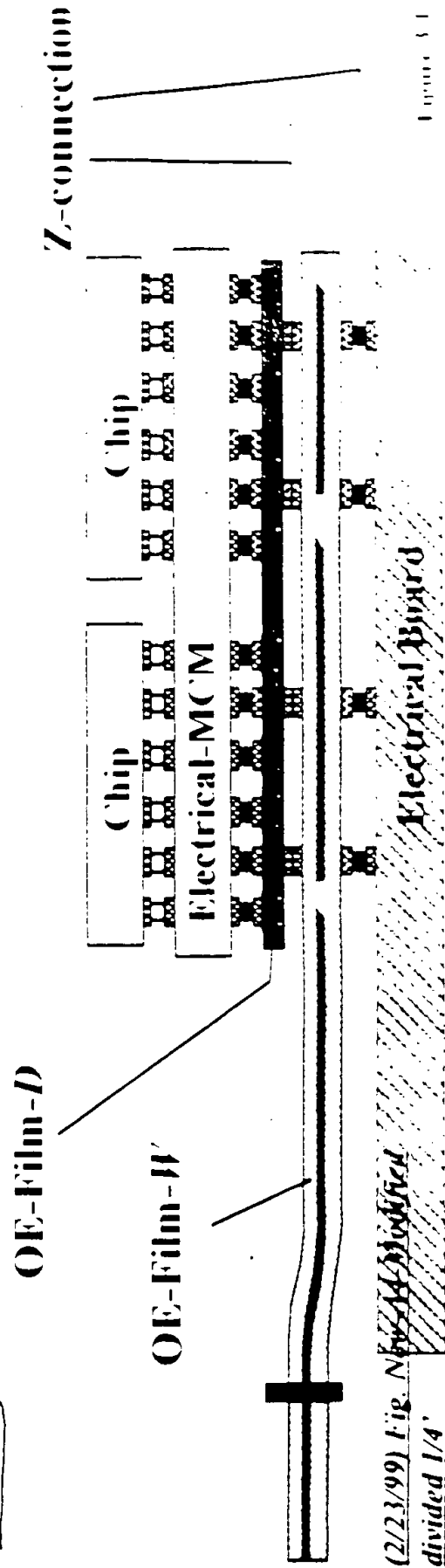


Fig. 119



(2/23/99) Fig. No. 14 Modified
divided 1/4'

Fig. 120

FUJITSU Computer Packaging Technologies, Inc. **FCPT**
FOLM with Optical Path Length Controller, Connector Buffer

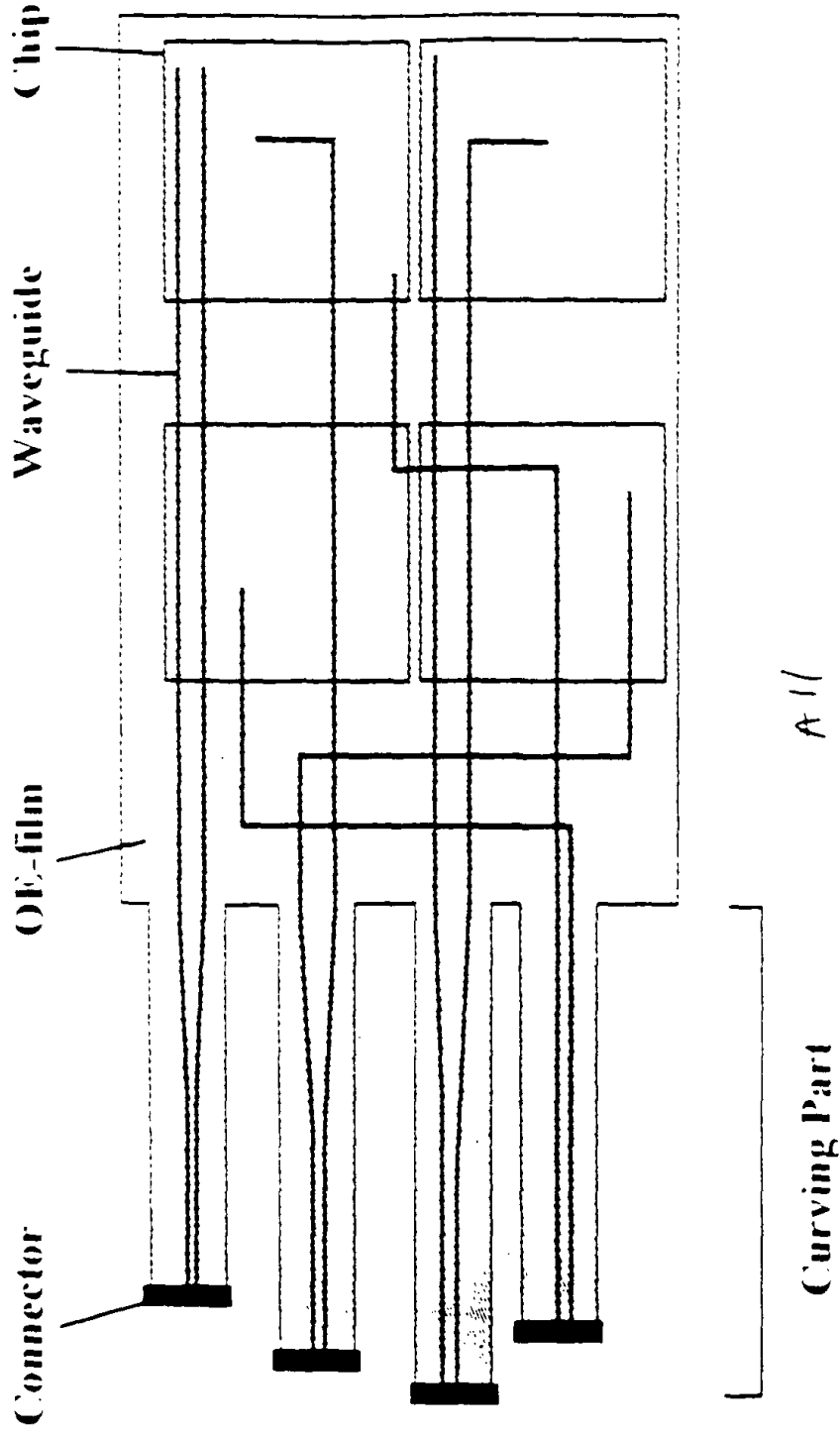


FIG. 121

(2/17/99) Fig. New-A4-Modified
 divided 2/4

FUJITSU Computer Packaging Technologies, Inc. **FCPT**
FOLM with Optical Path Length Controller, Connector Buffer

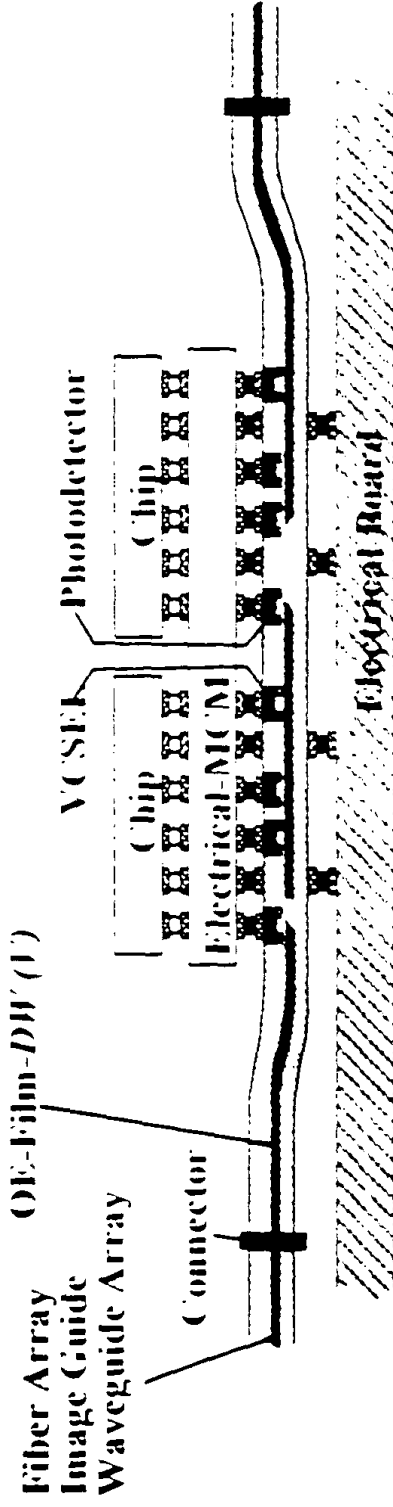


FIG. 123

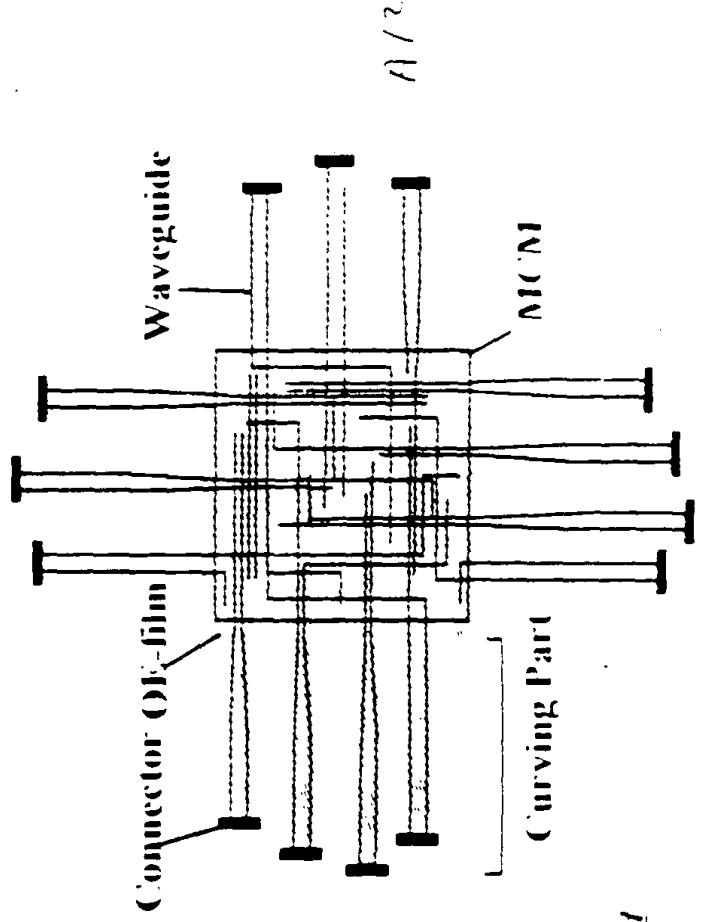
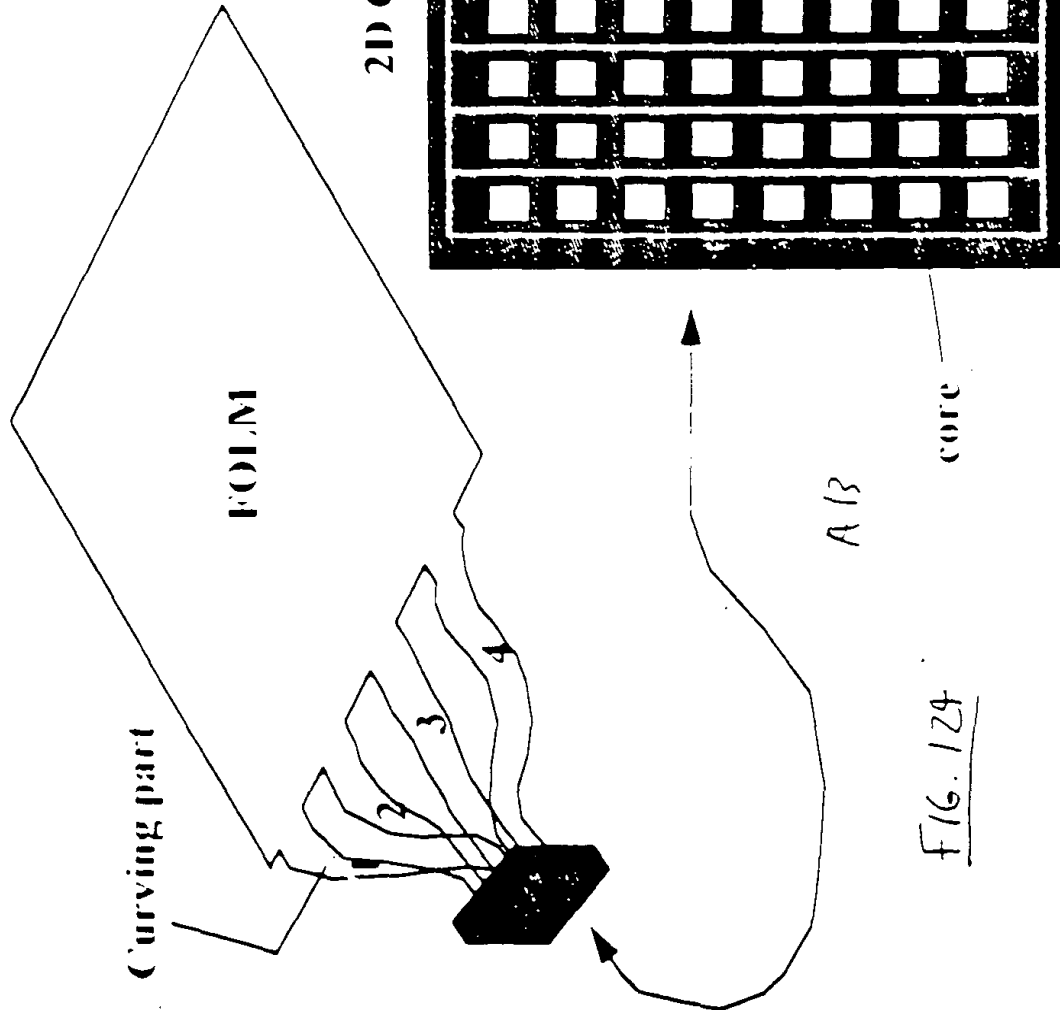


FIG. 122

(2/23/99) Fig. New-A4-Modified
 divided 2/4'

FOIM with 2D Waveguide Connector



(2/23/99) Fig. New-A4-Modified
divided 3/4

(for Single-layer waveguide) (for 2 layer waveguide) (for 3 layer waveguide)

FOI.M: High-Speed Option

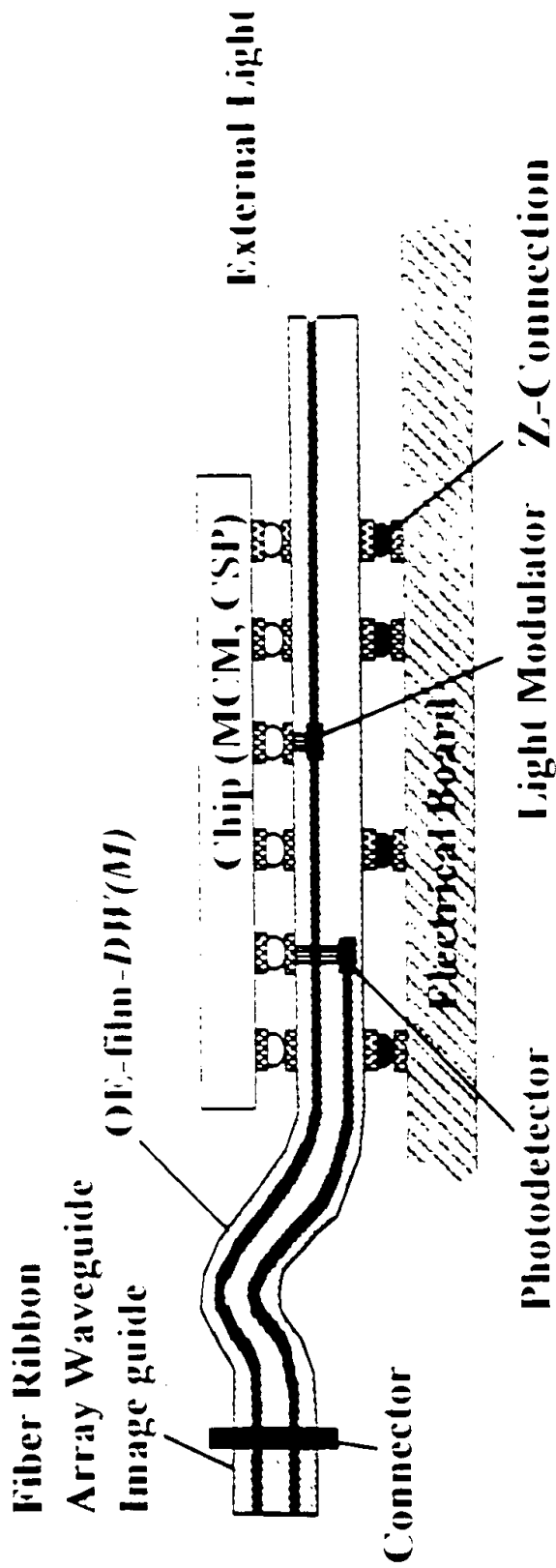


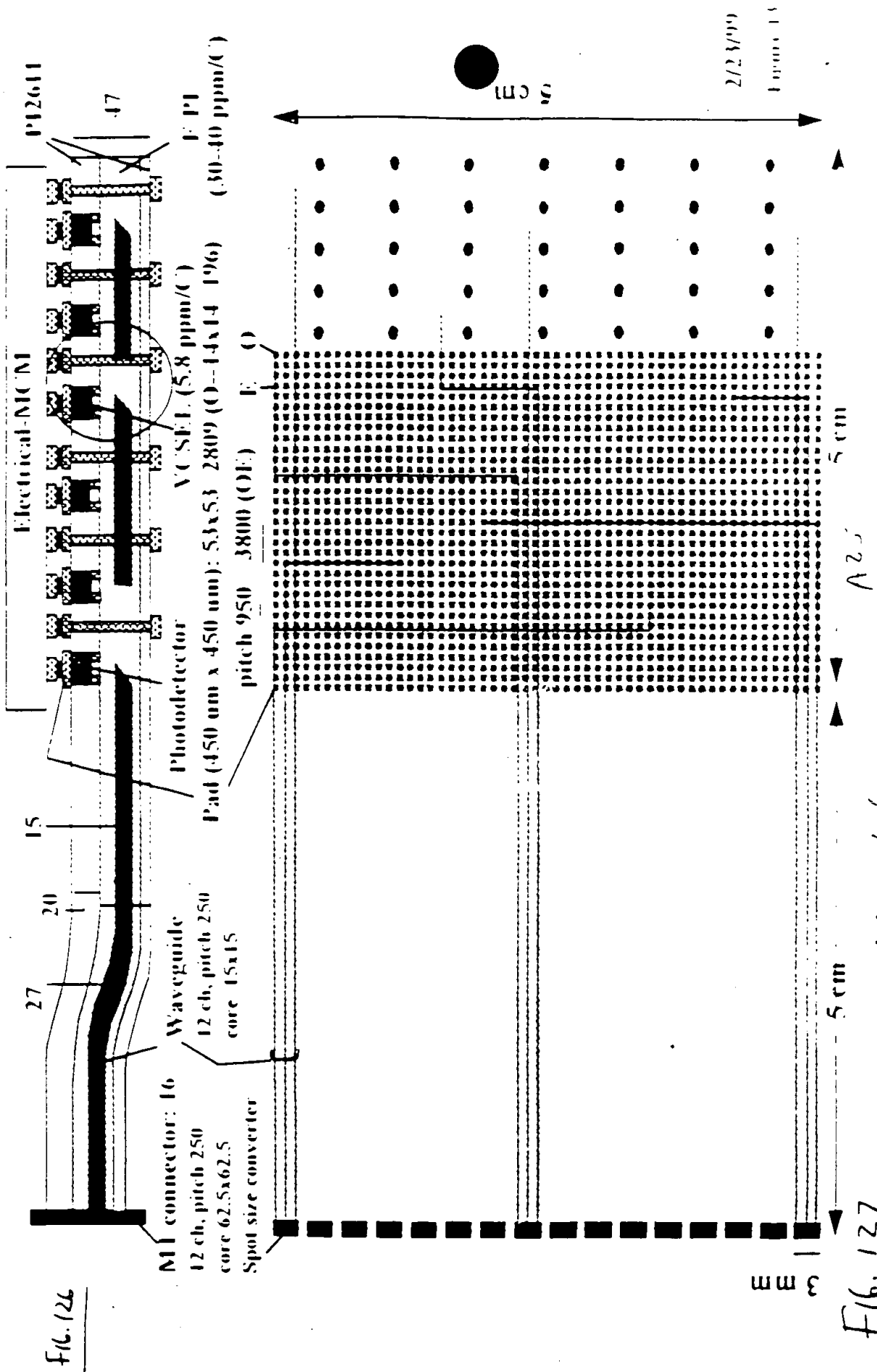
Fig. 125

A 14

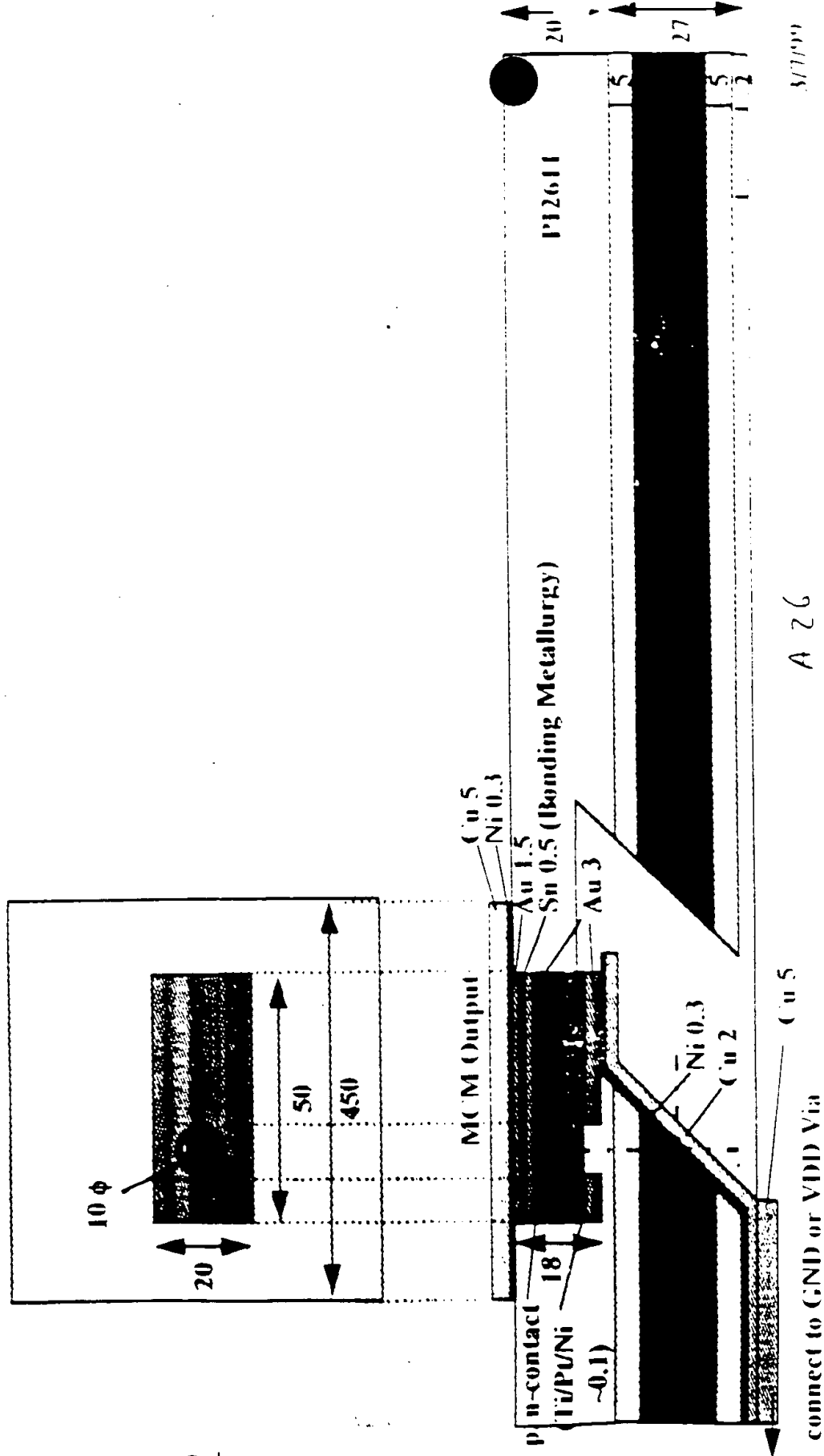
FOILM Structure Example (Overall)

Through put: 1.5 pbs x 196 ch Assume SSN MCM Size is 5 cm x 5 cm

Unit: um



FOILM Structure Example (VCSEL part)



Unit : um

FIG. 128

OE-film: OE-IP, OE-Film-MCM

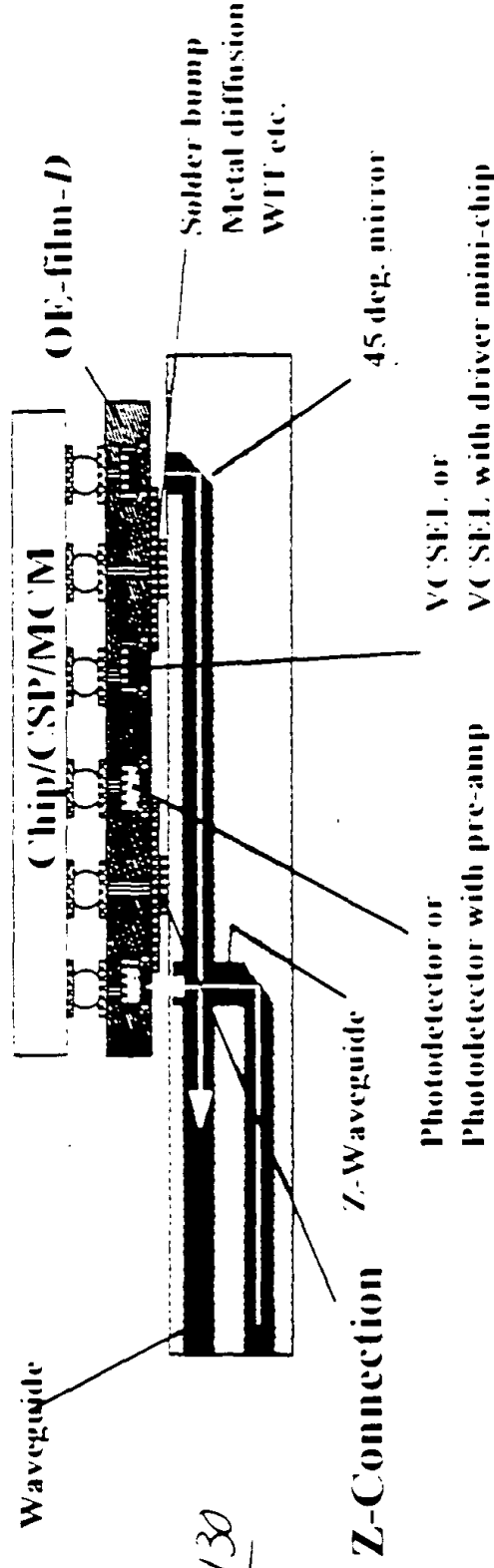


Fig. 130

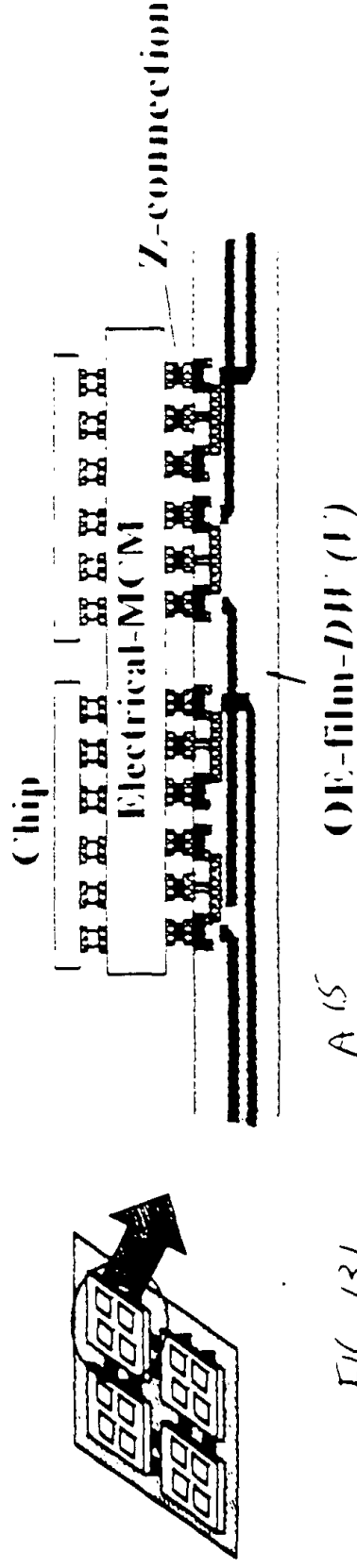
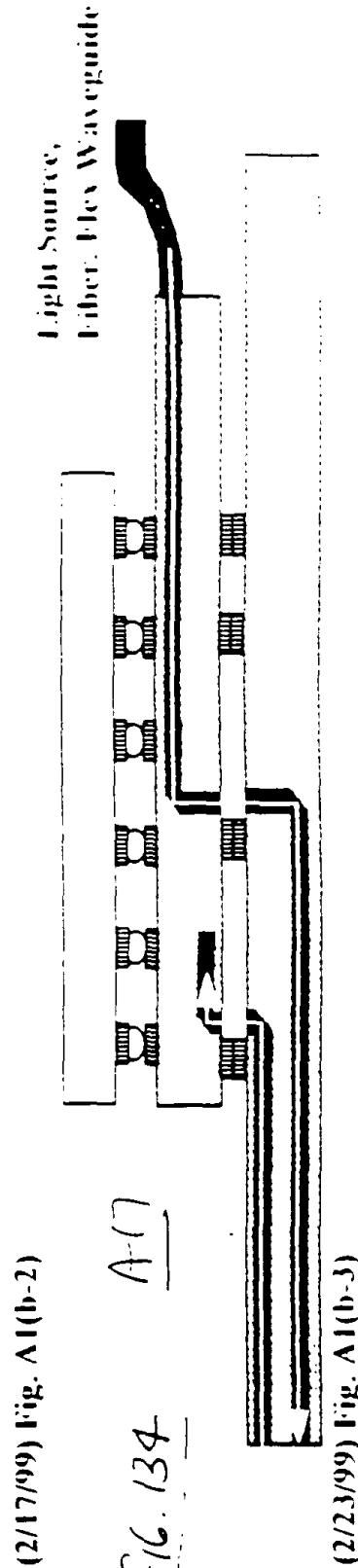
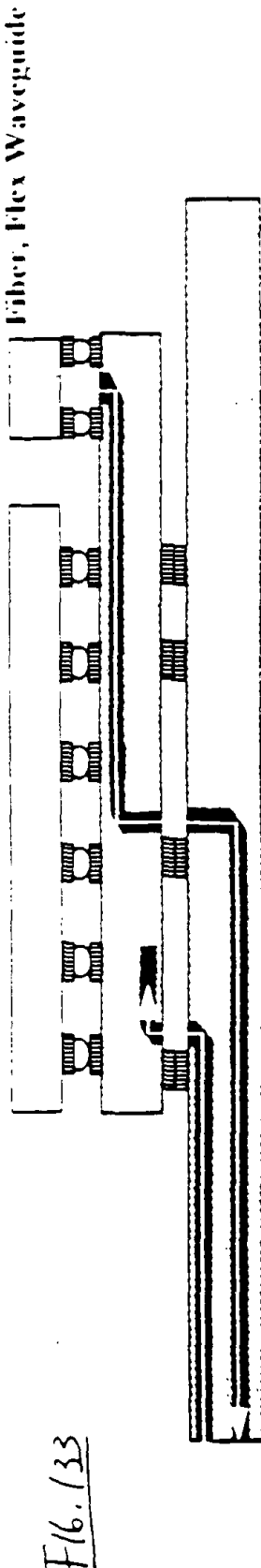
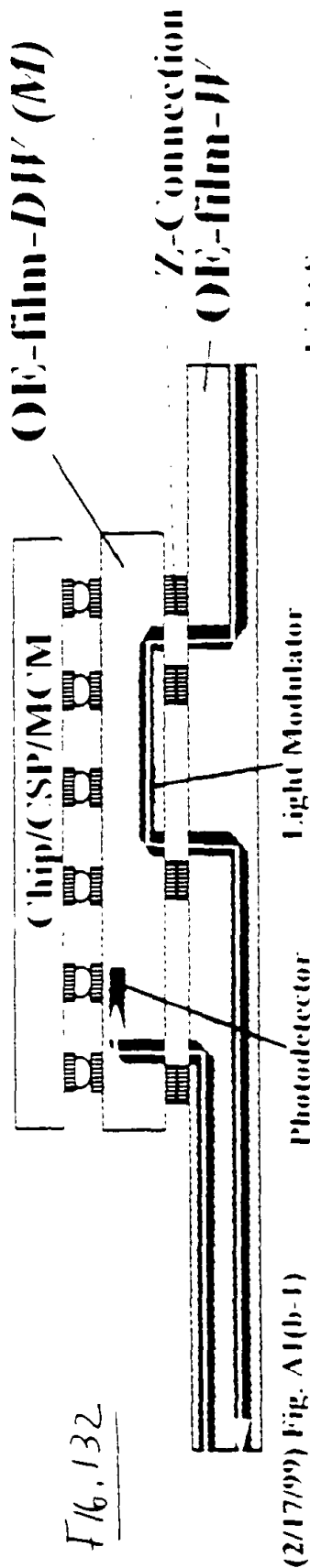


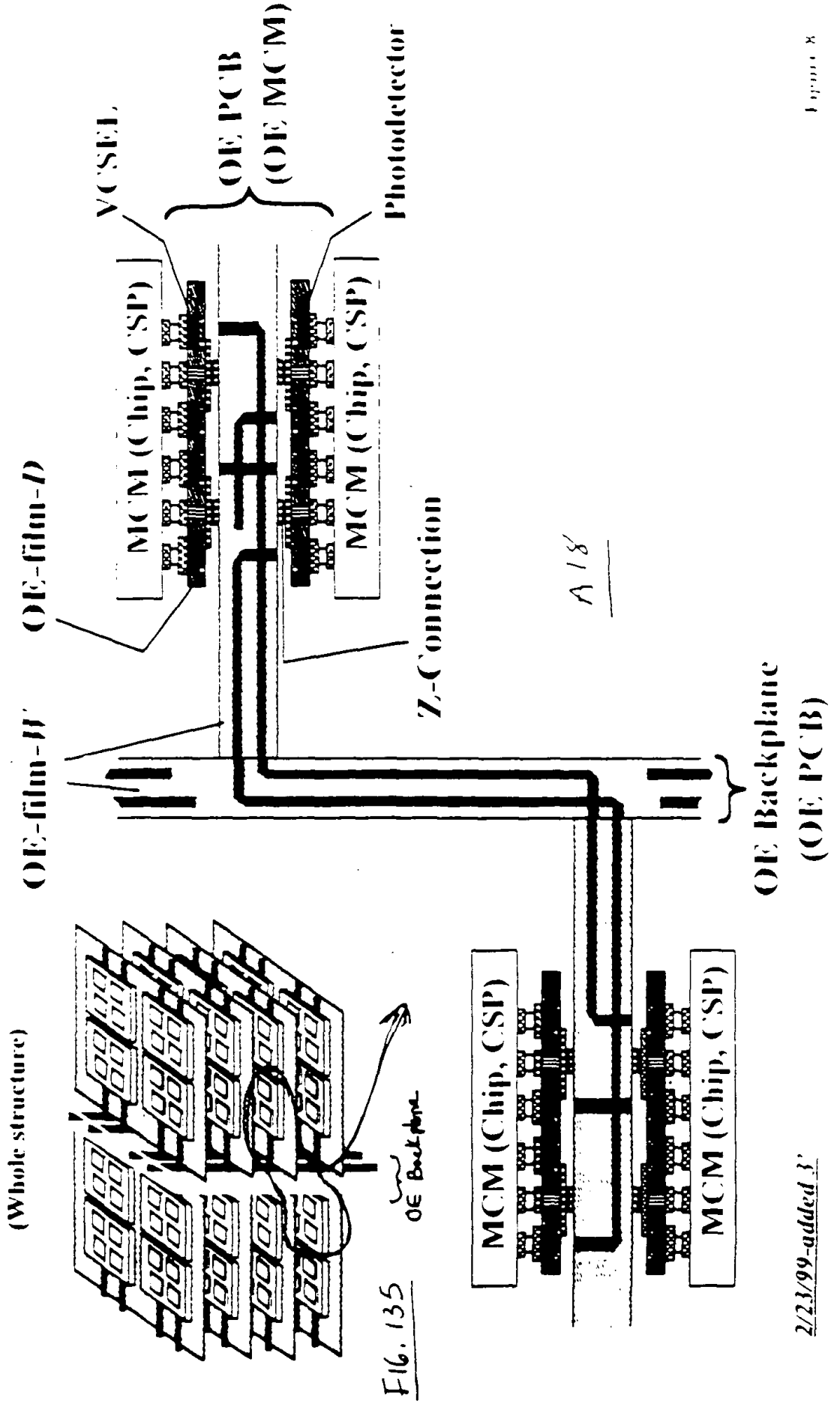
Fig. 131

(2/23/99) Fig. New-A1-Modified

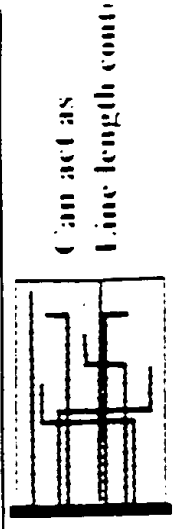
OE-film: Light Modulator Transmitters



OE-film: Both-Side Packaging

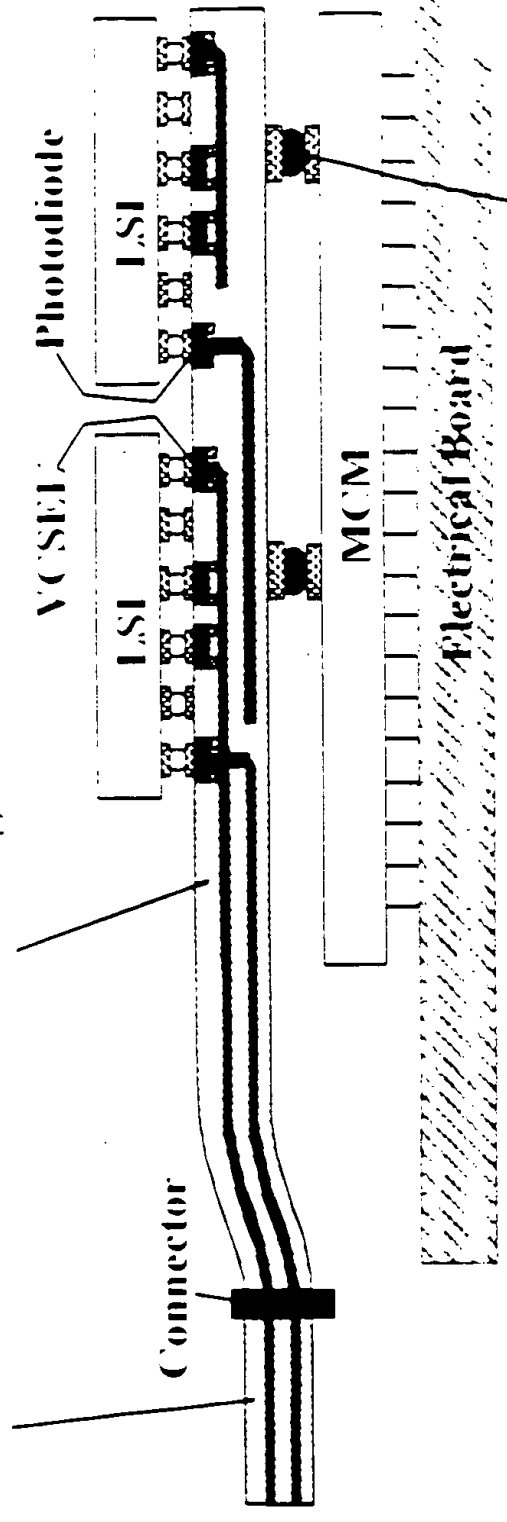


Direct Jump from LSI



Fiber Ribbon Film Waveguide with Device Integration

Fig. 136



Z-Connection

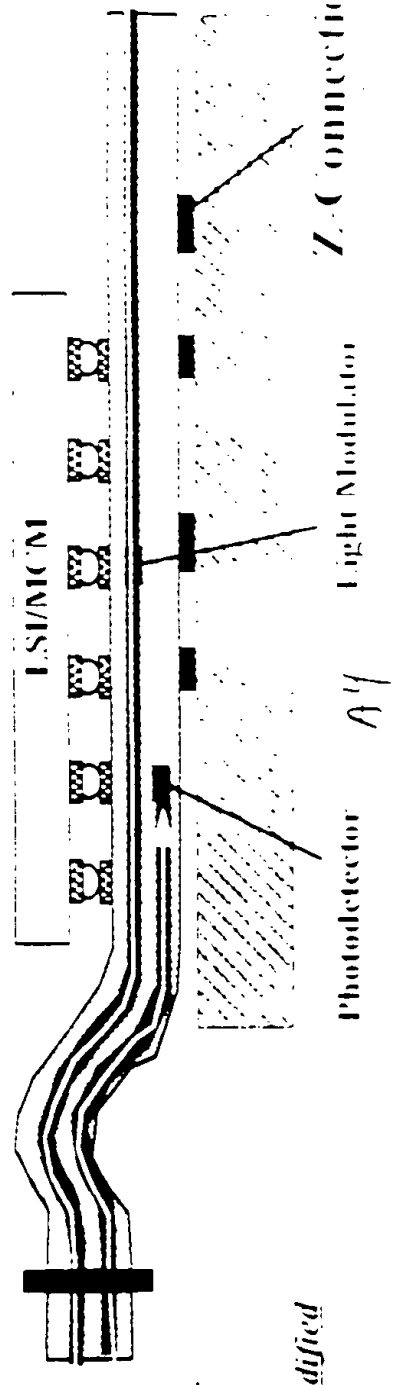
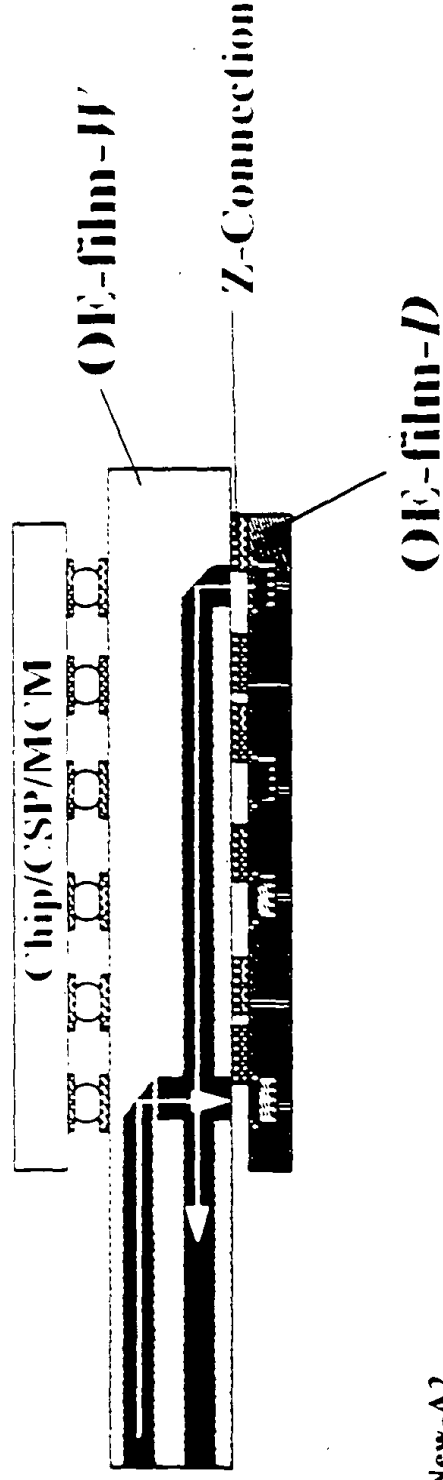


Fig. 137

Fig. New-A4-Modified

OE IP is Placed on the Oposit Side



(2/23/99) Fig. New-A2

FIG. 138

A20

OE MCM

OE-MCM

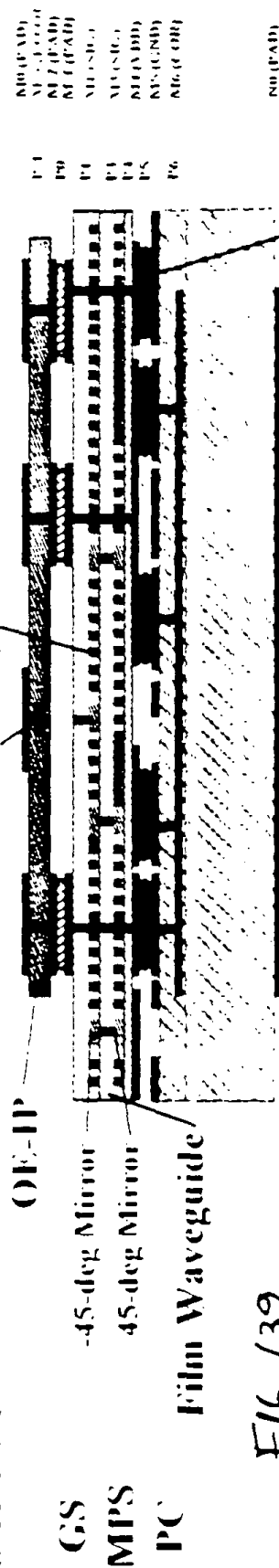


Fig. 139

Z-Connection

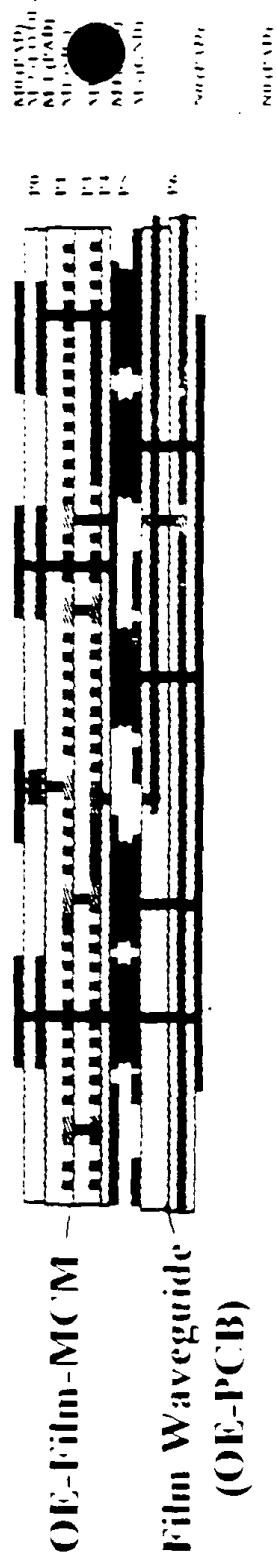


Fig. 140

Fig. A5-Modified

AS

OE-film: Smart Pixel

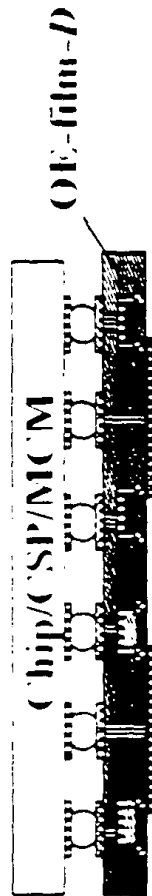


FIG. 141



FIG. 142

A16

OE-Film/OE-Film Stack --- Back-Side Connection

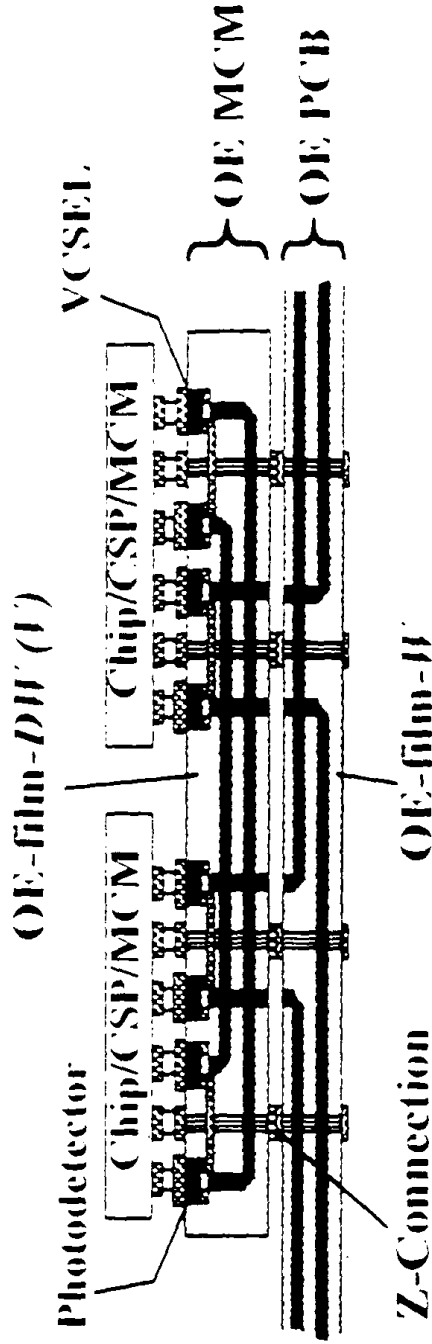
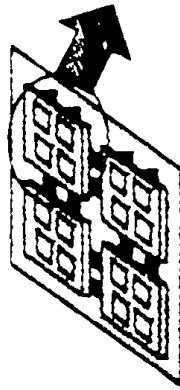
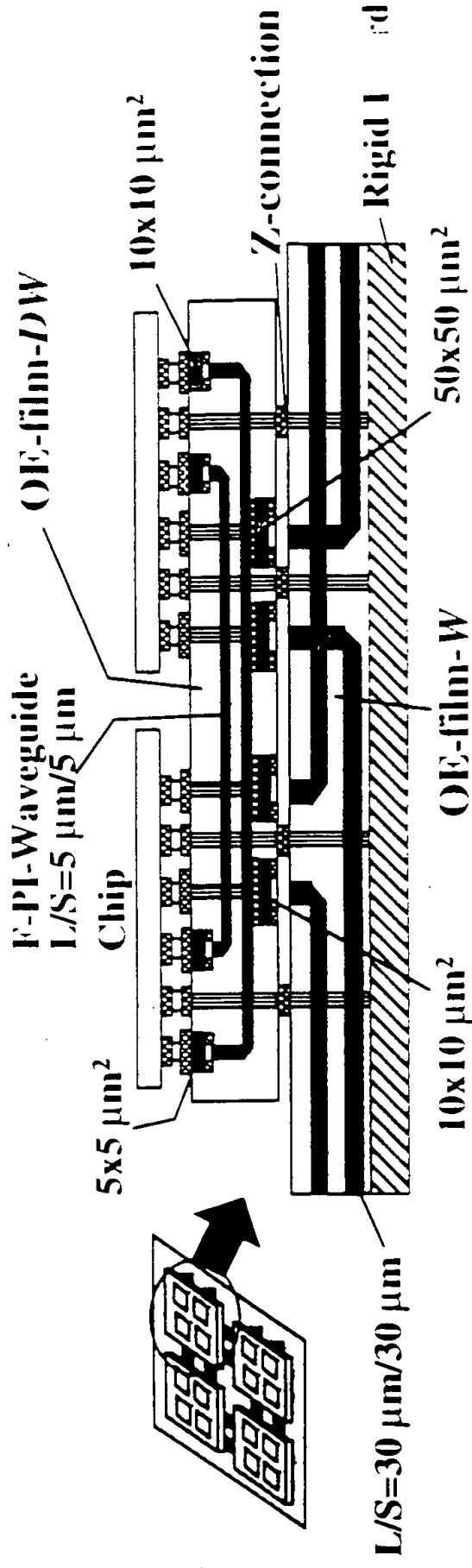


FIG. 143

A19

FUJITSU Computer Packaging Technologies, Inc. **FCPT**
OE-Film/OE-Film Stack --- Back-Side Connection



DI

Fig. 144

Fig. 3/18/99-1

DI 3/18/99

OE-MCM/OE-Bord Stack

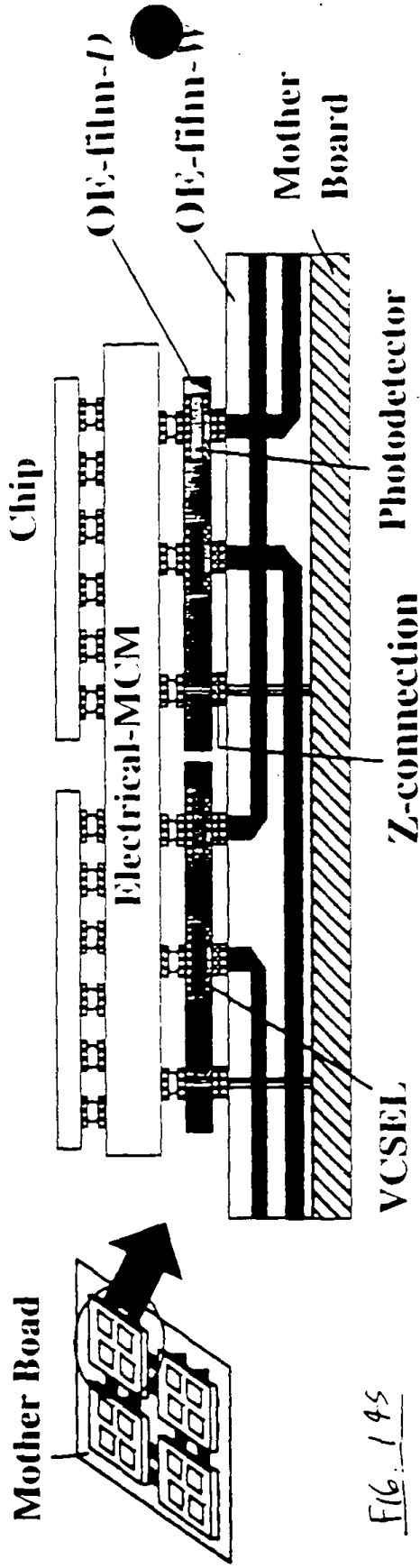


Fig. 145

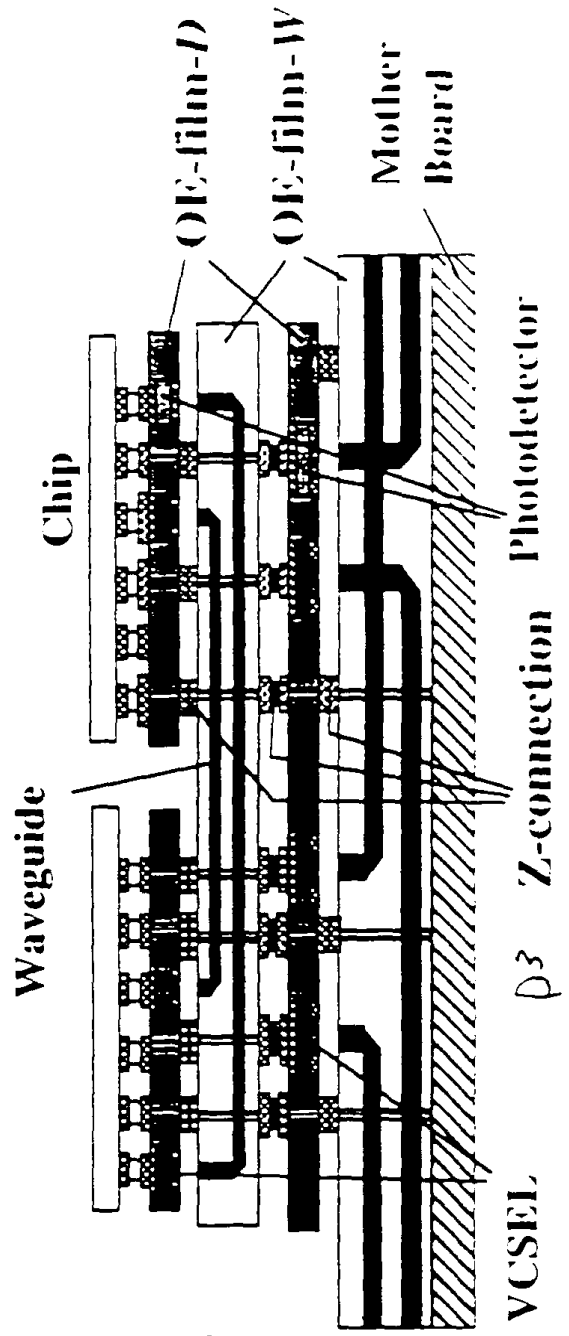
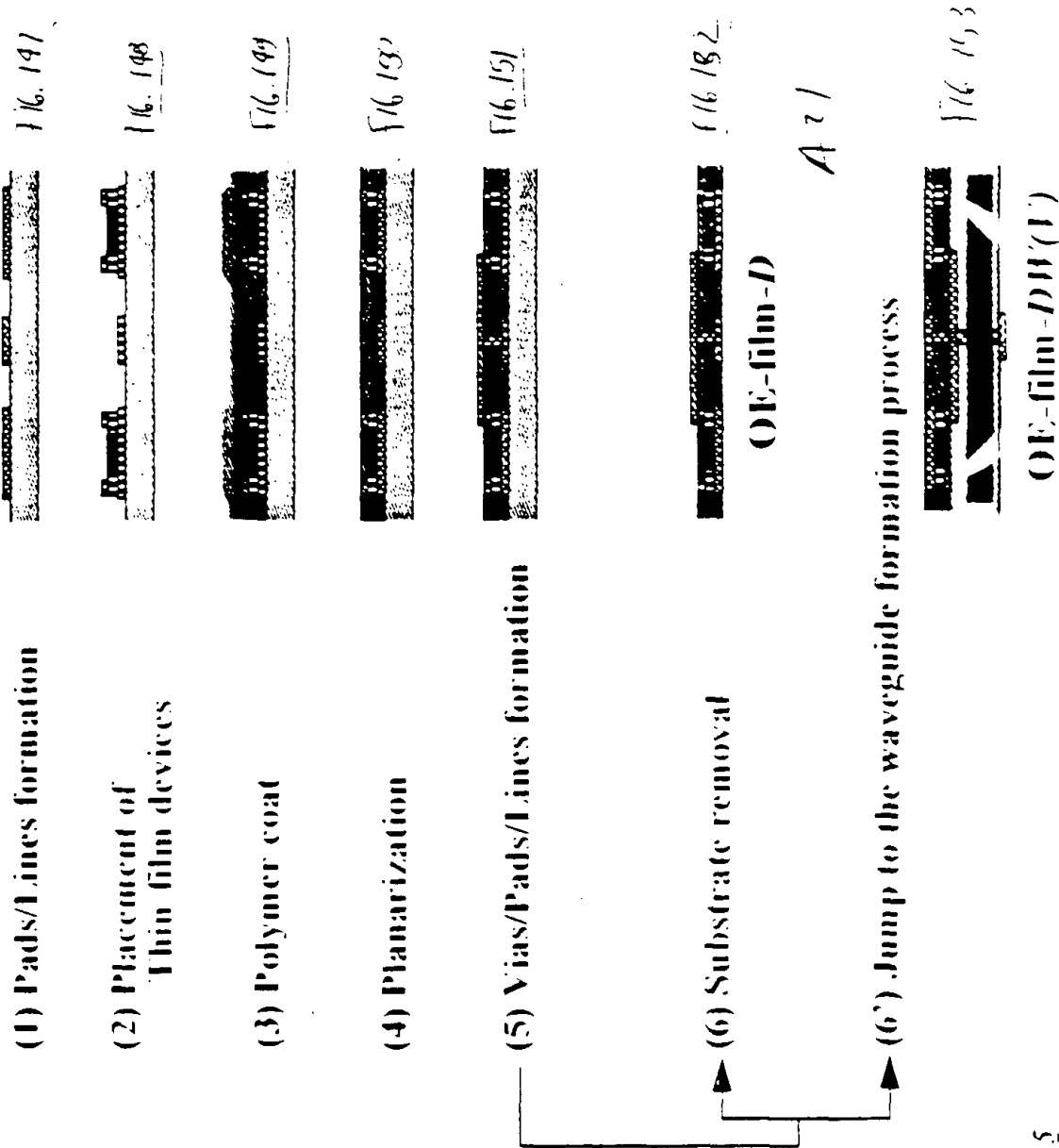


Fig. 3/19/99-1

Device Integration Process



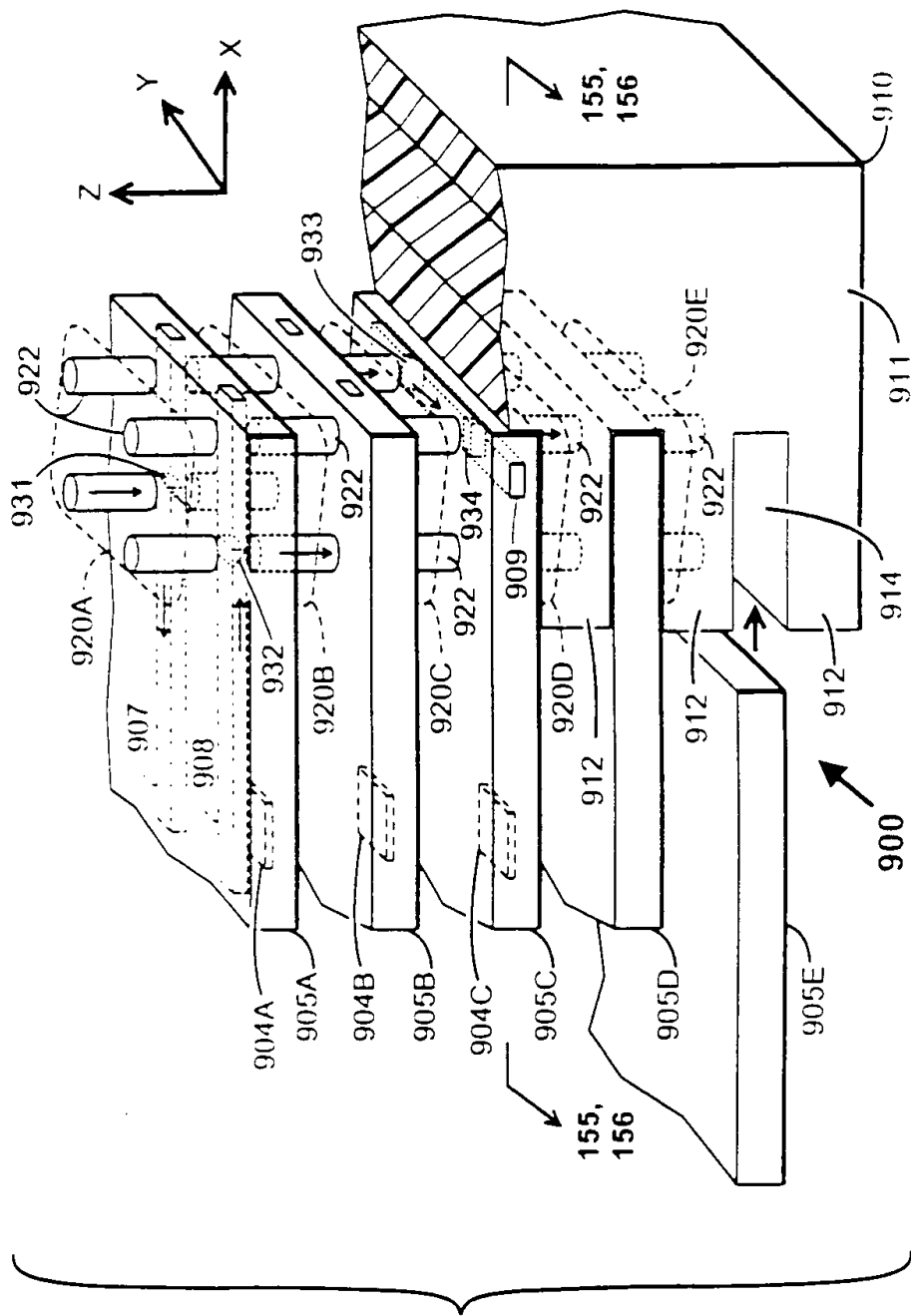


FIG. 154

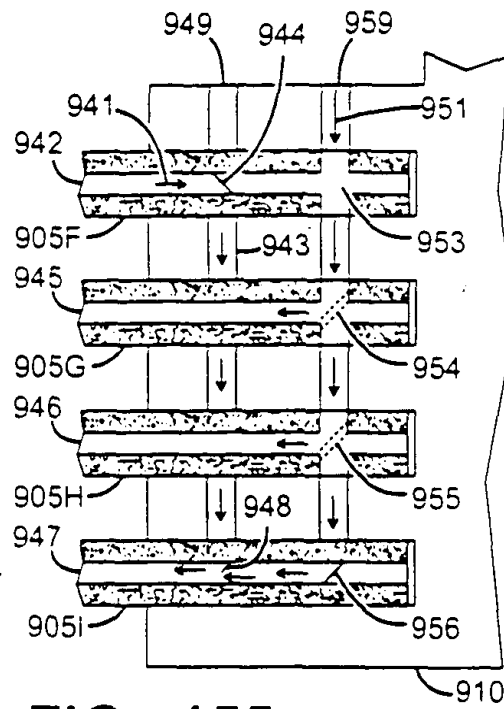


FIG. 155

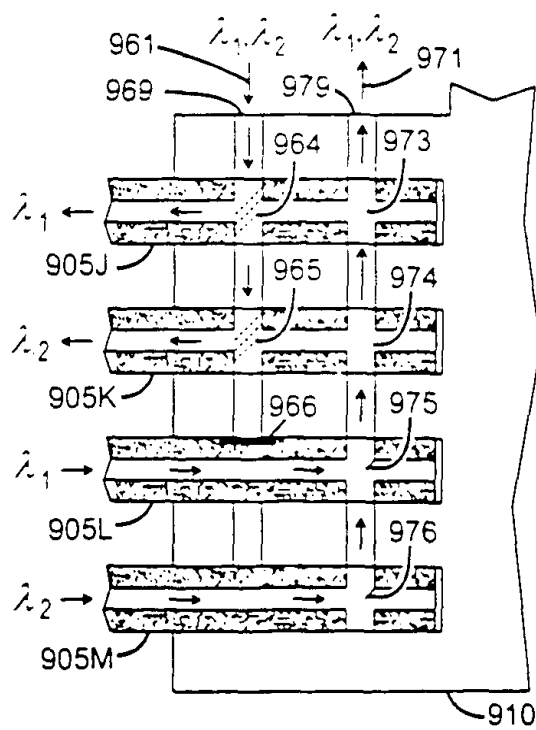


FIG. 156-1

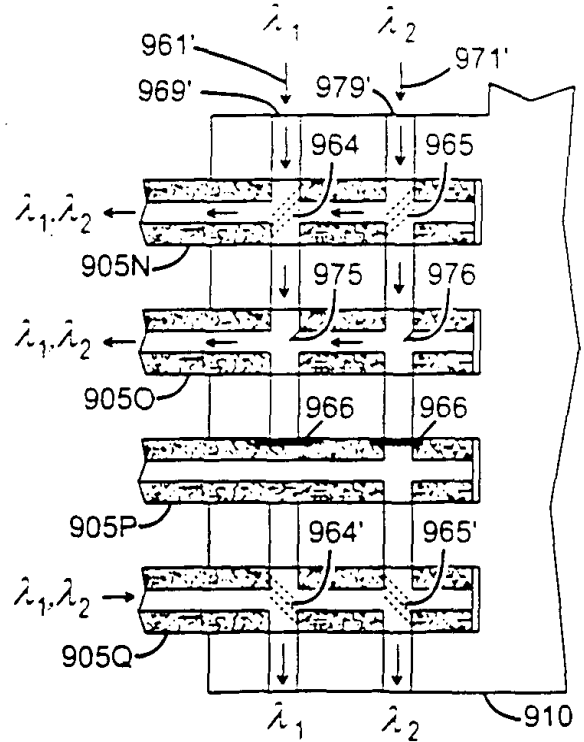


FIG. 156-2

1/XX

FIG. 157

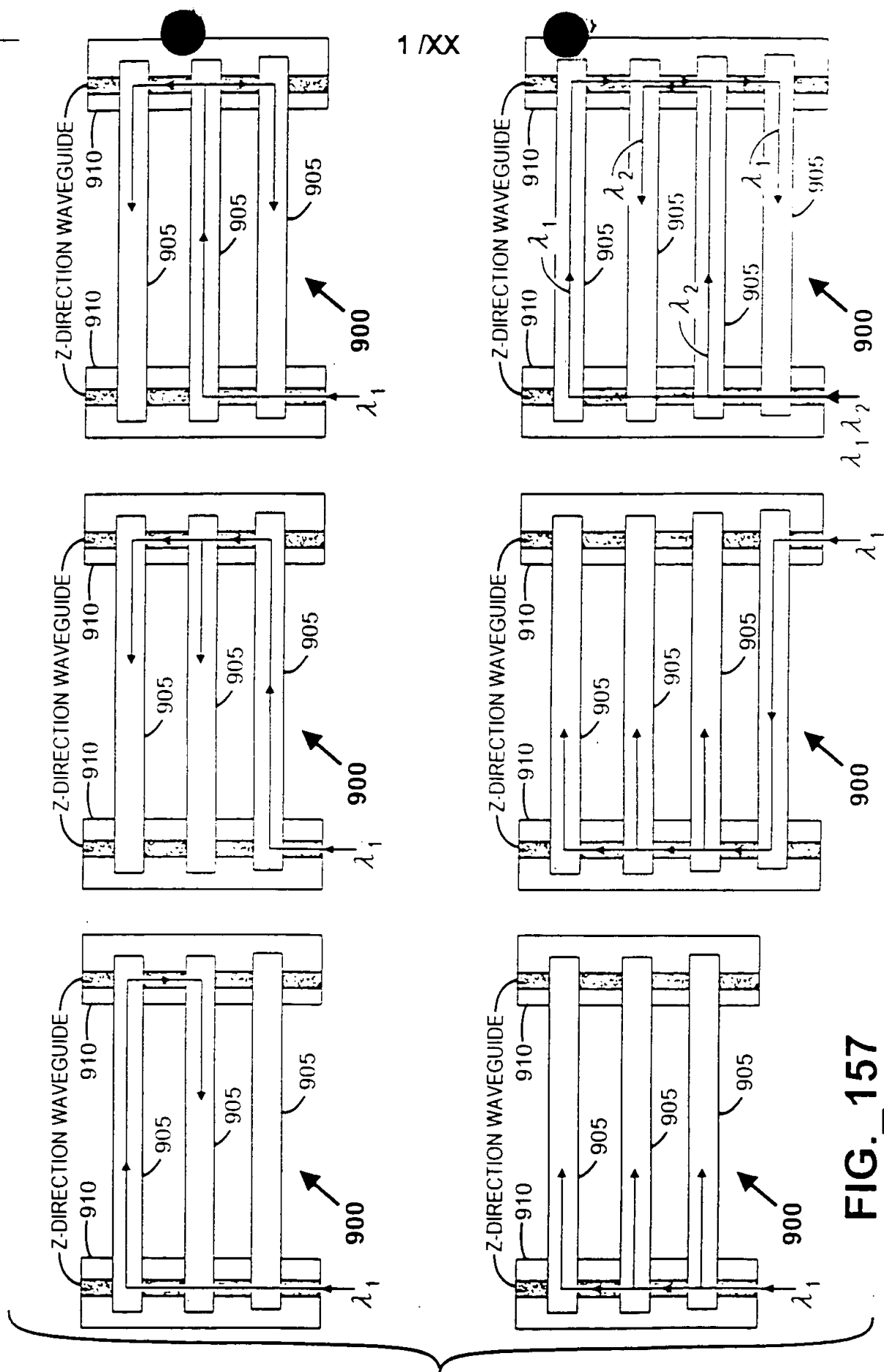


FIG. 157

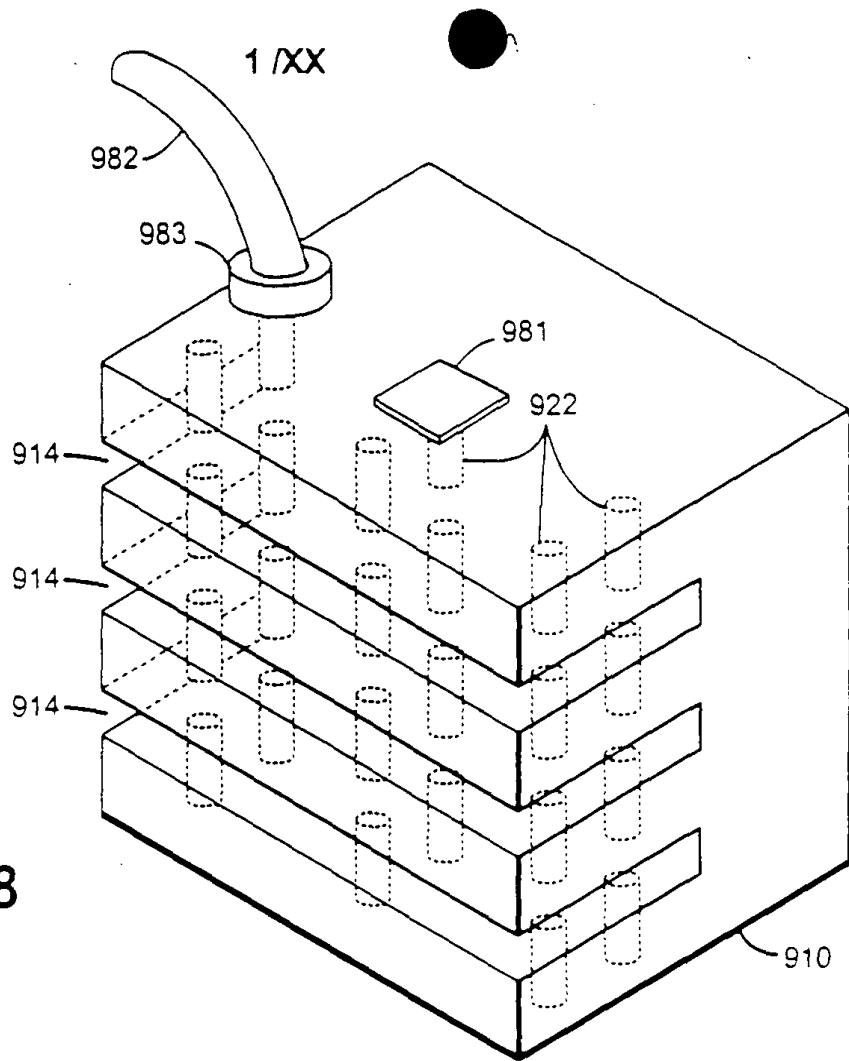


FIG._158

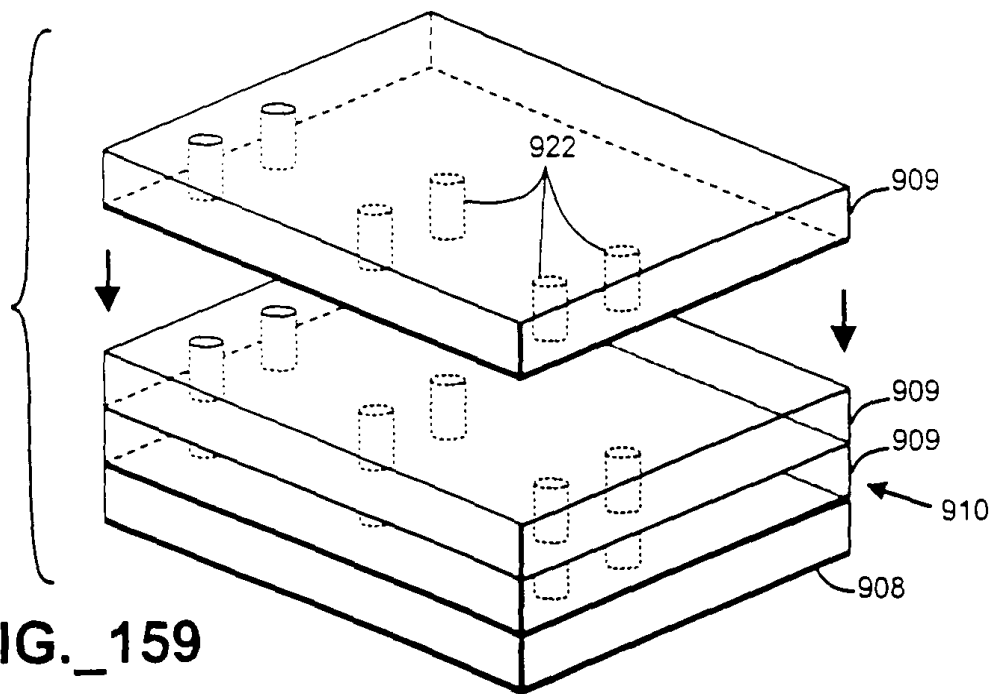


FIG._159

09767582.012201
T02270" 28549460

FIG._160

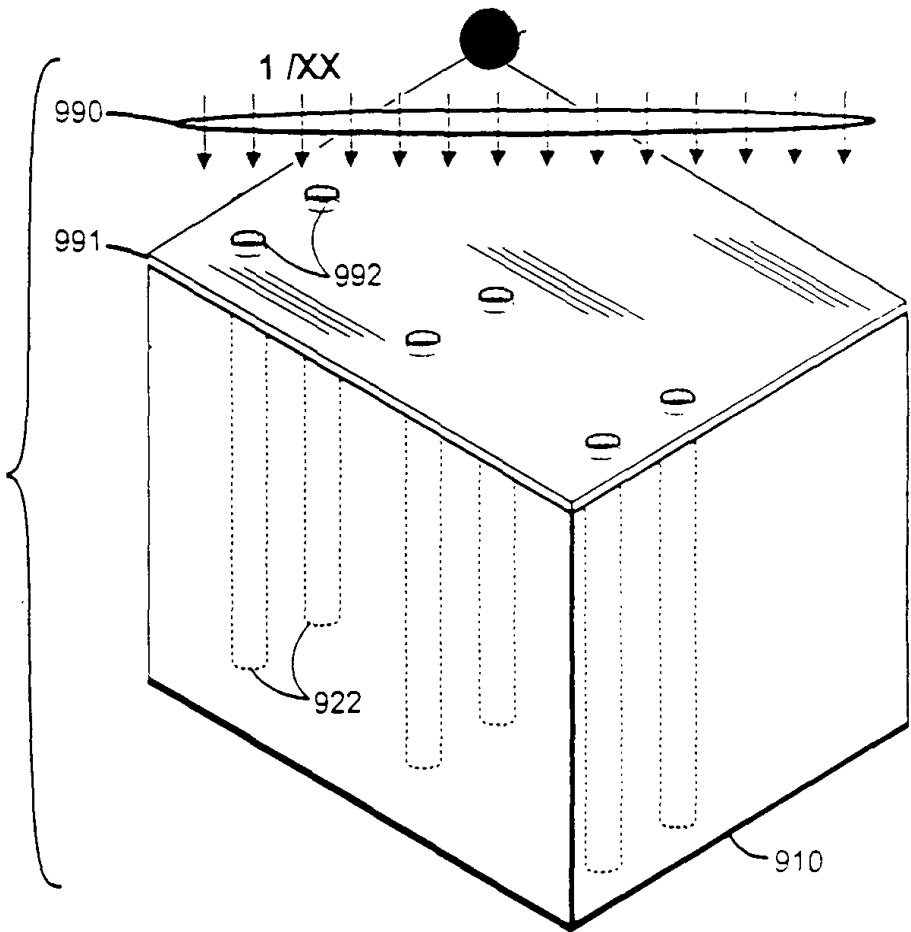
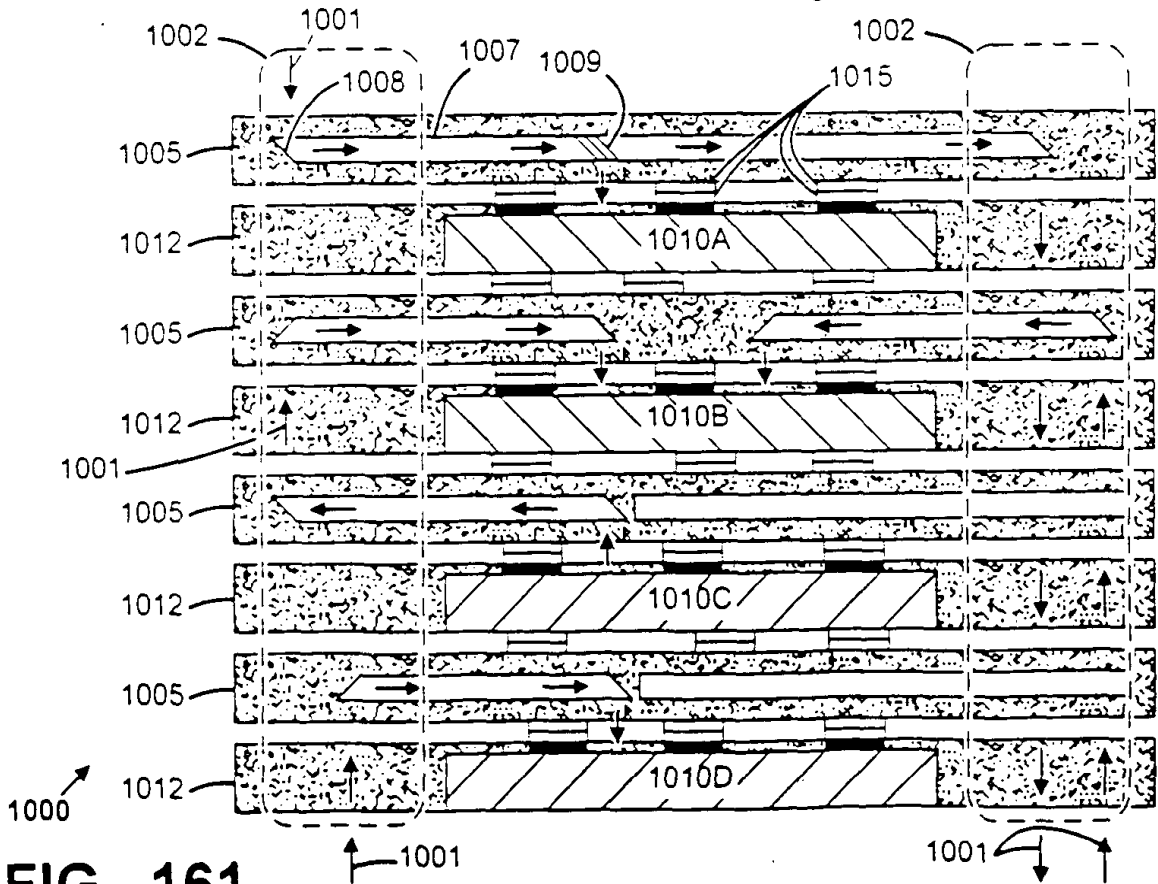
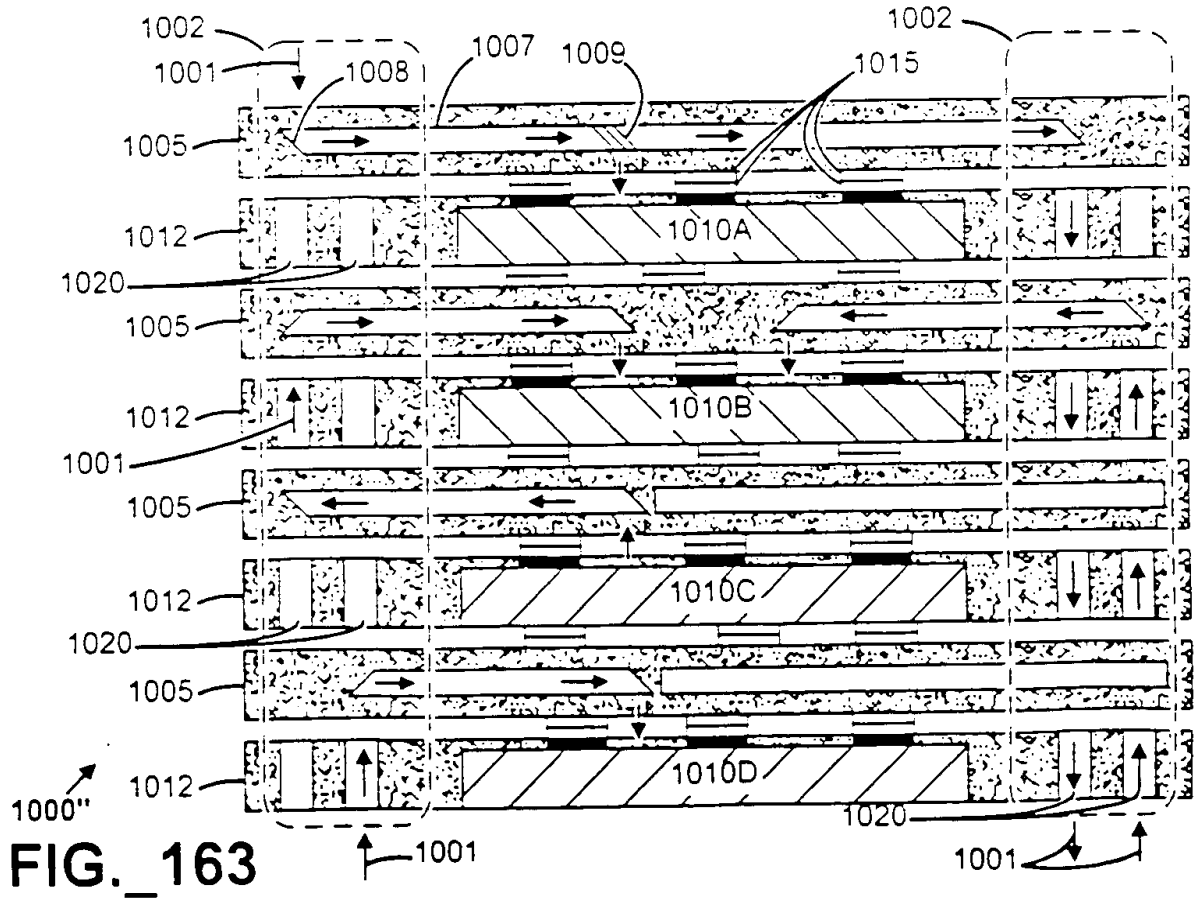
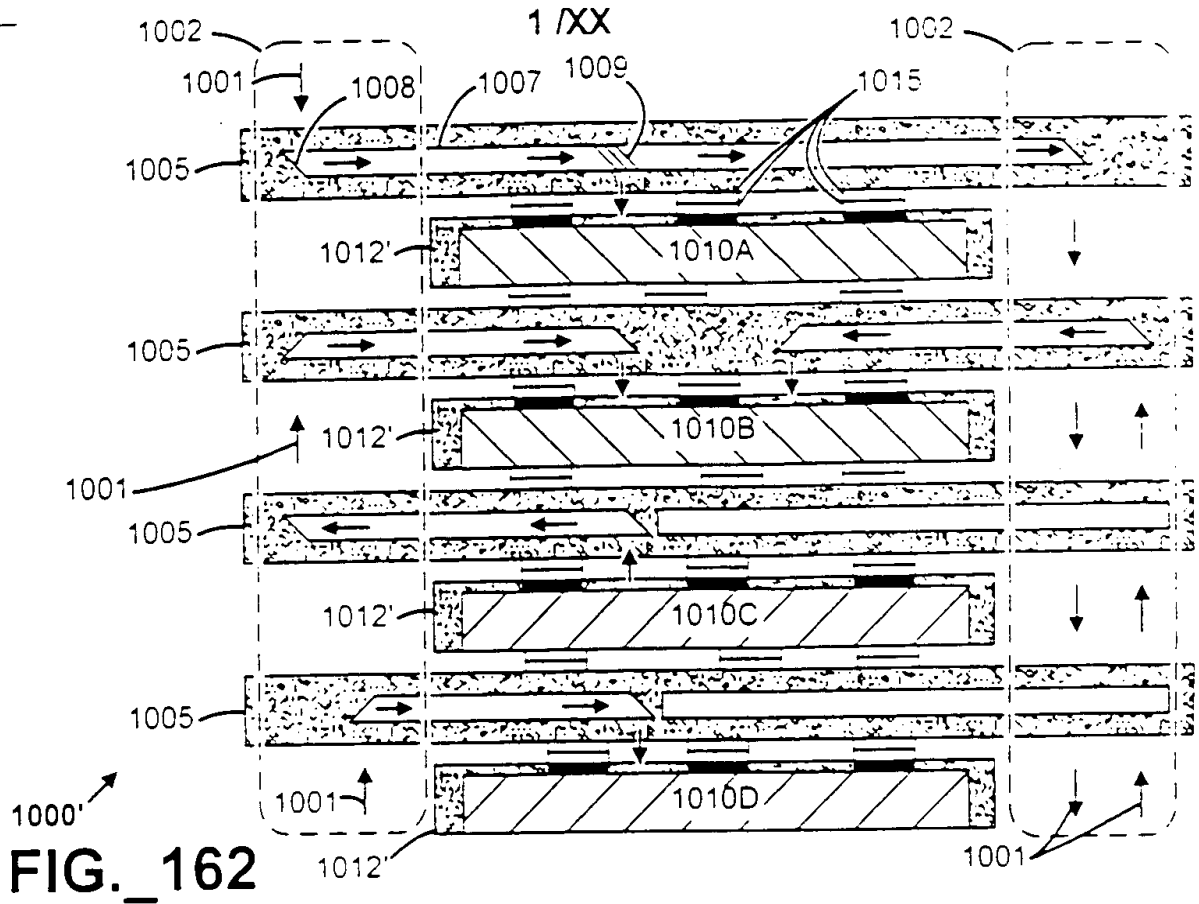
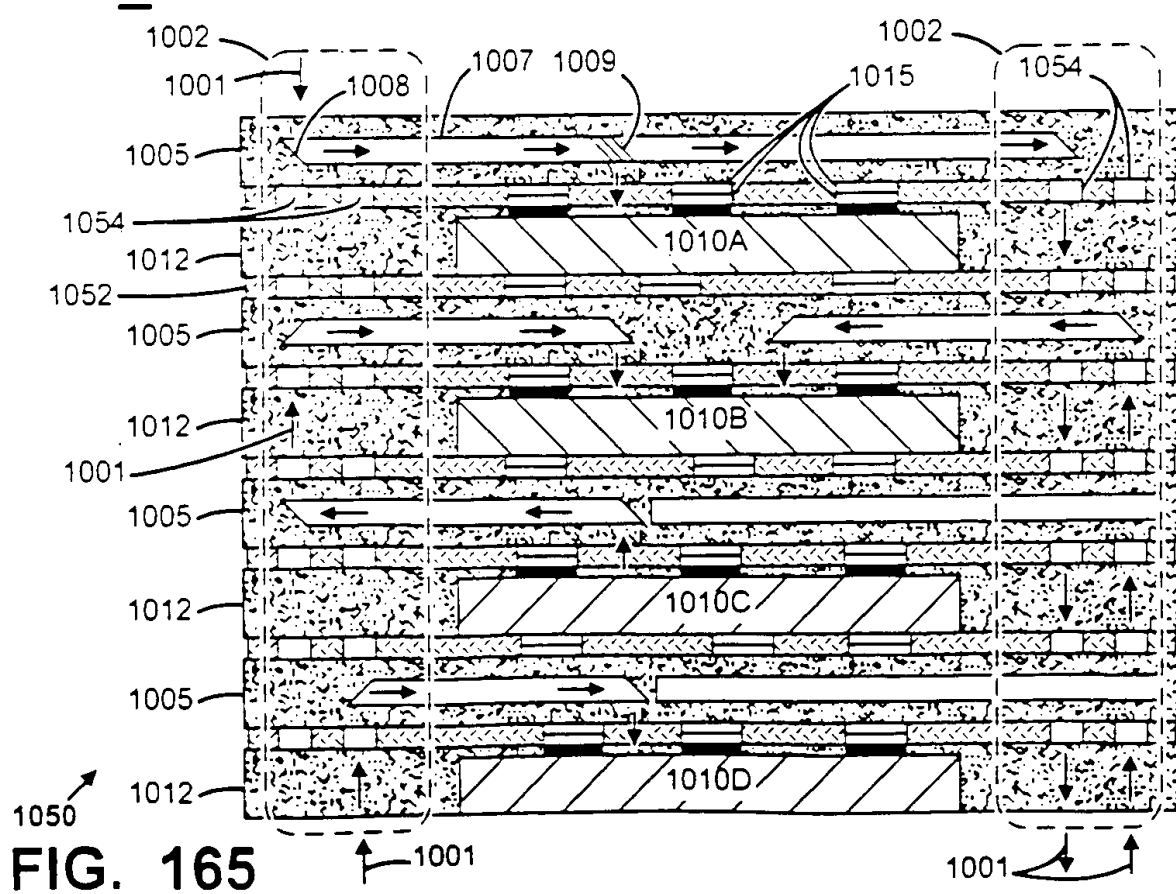
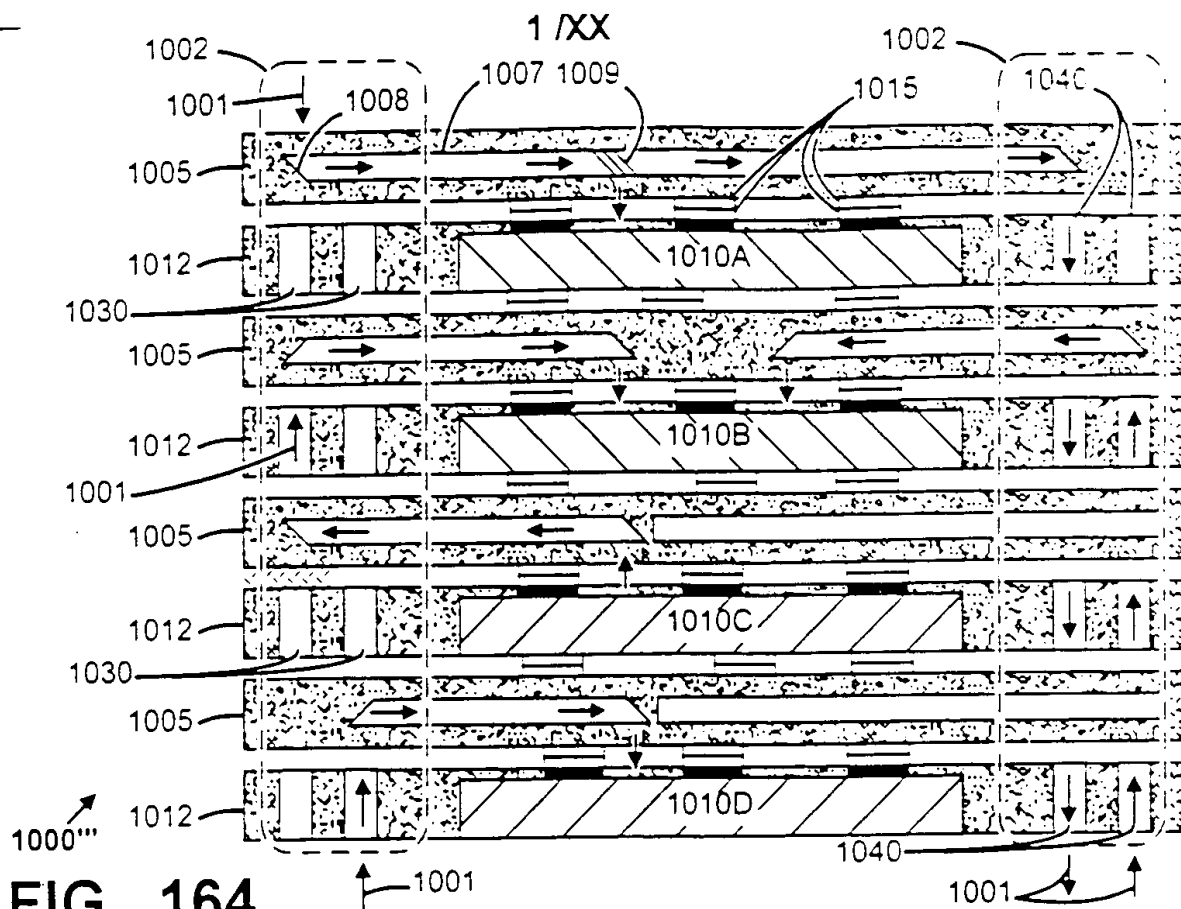


FIG._161







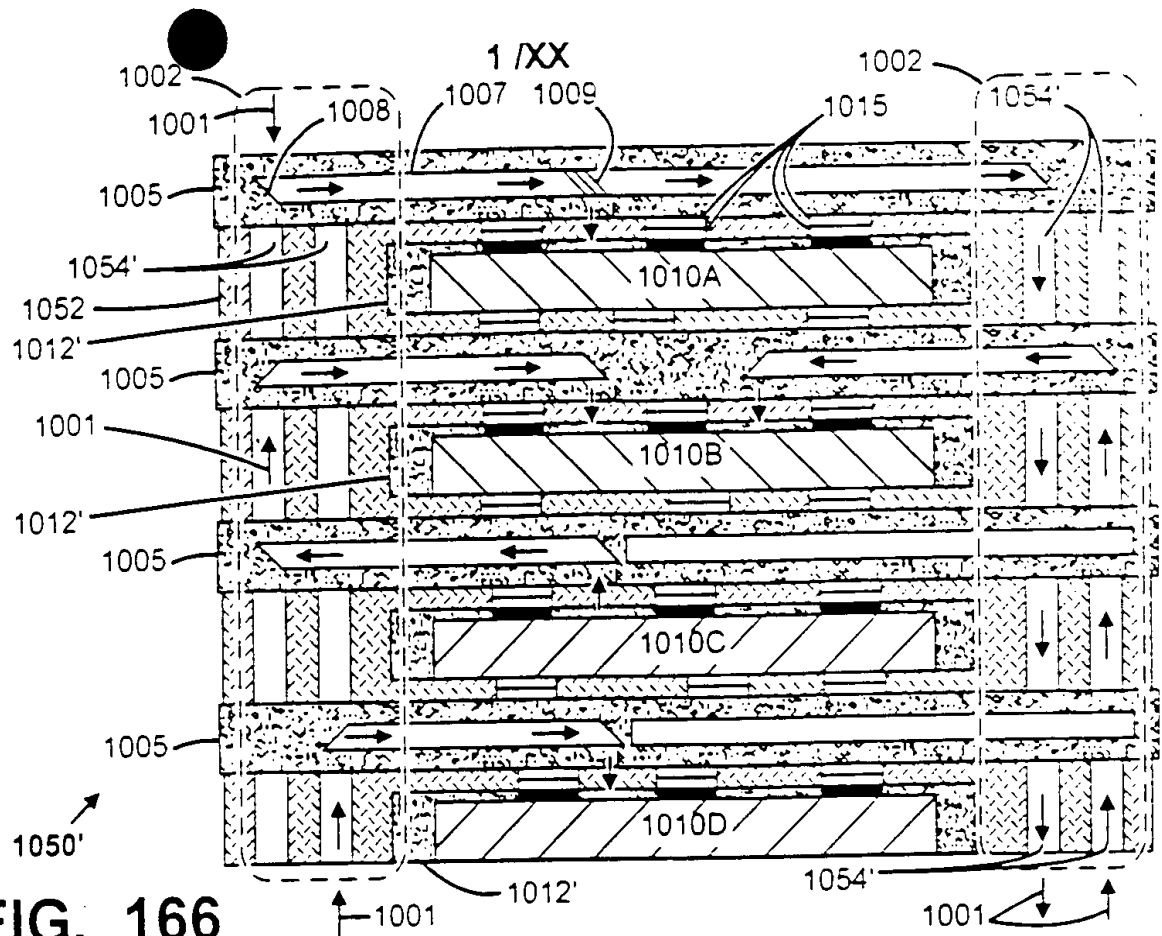


FIG. 166

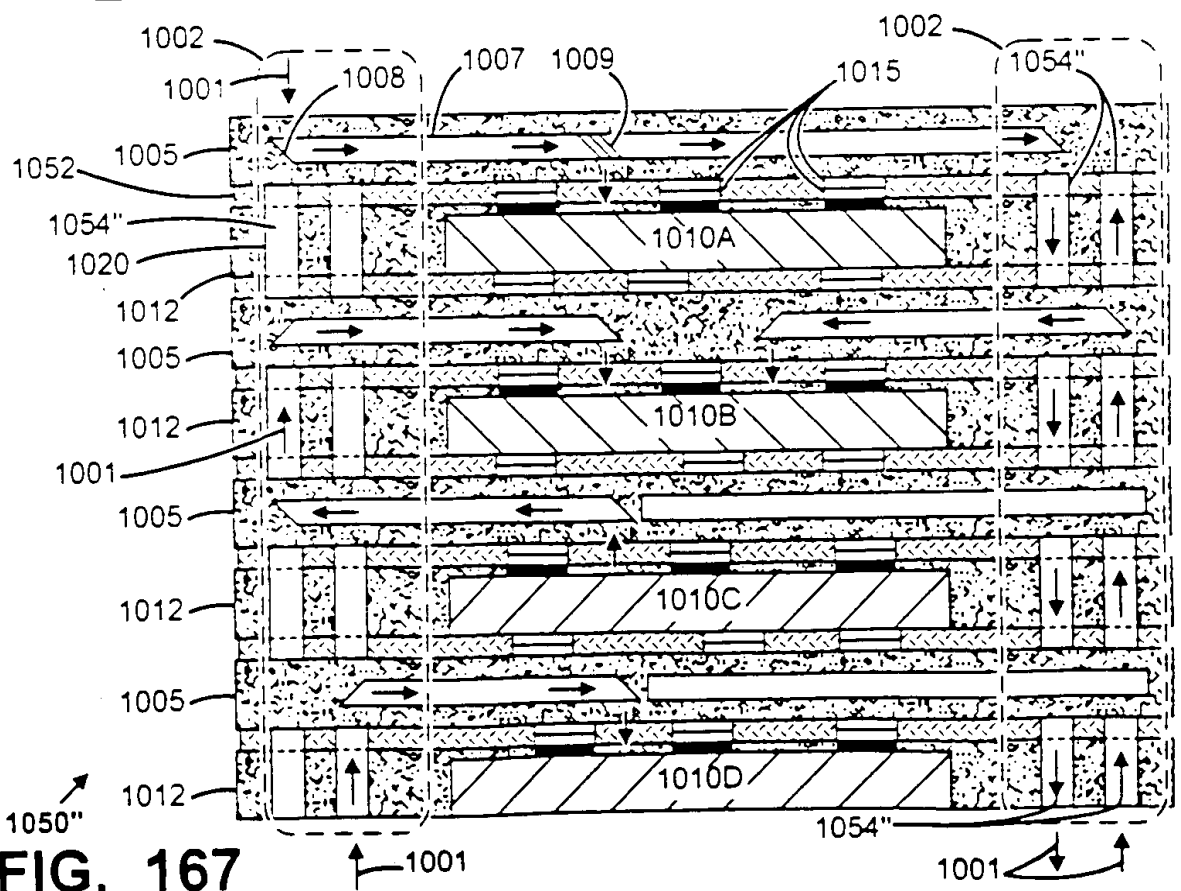


FIG. 167



1/XX

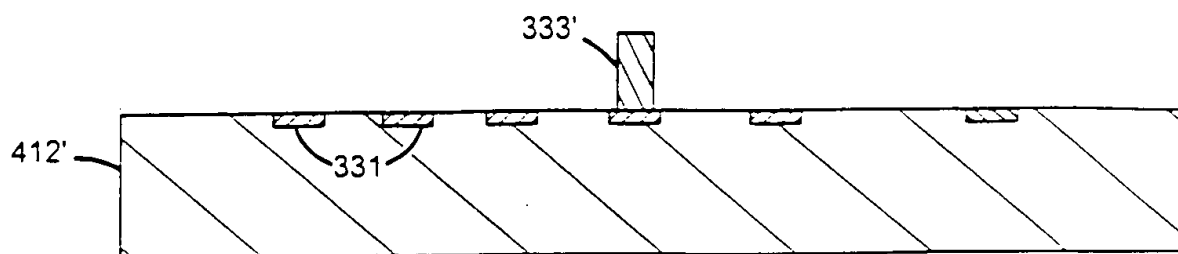


FIG._170

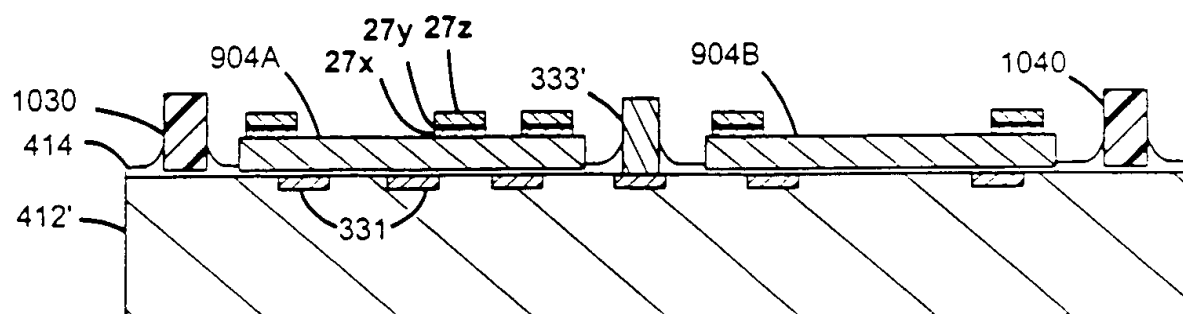


FIG._171

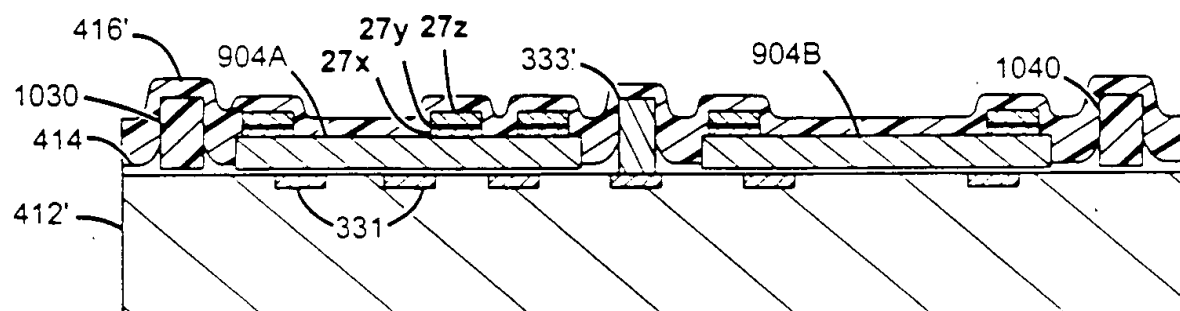


FIG._172

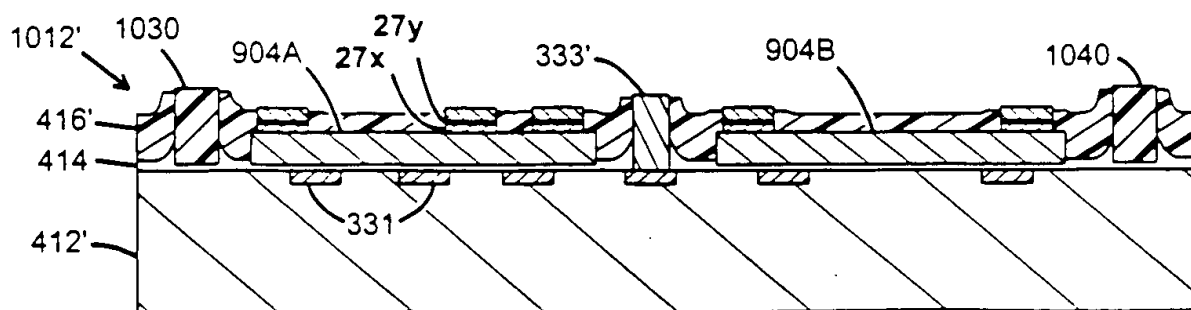


FIG._173

T02210-202409260

1/XX

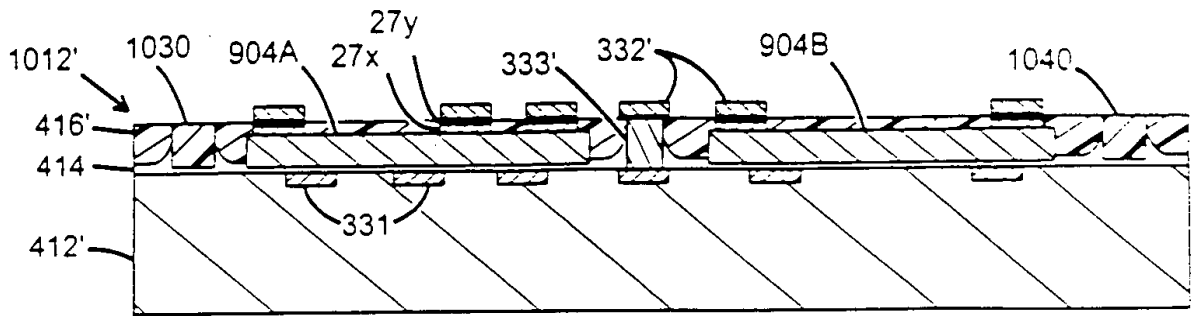


FIG._174

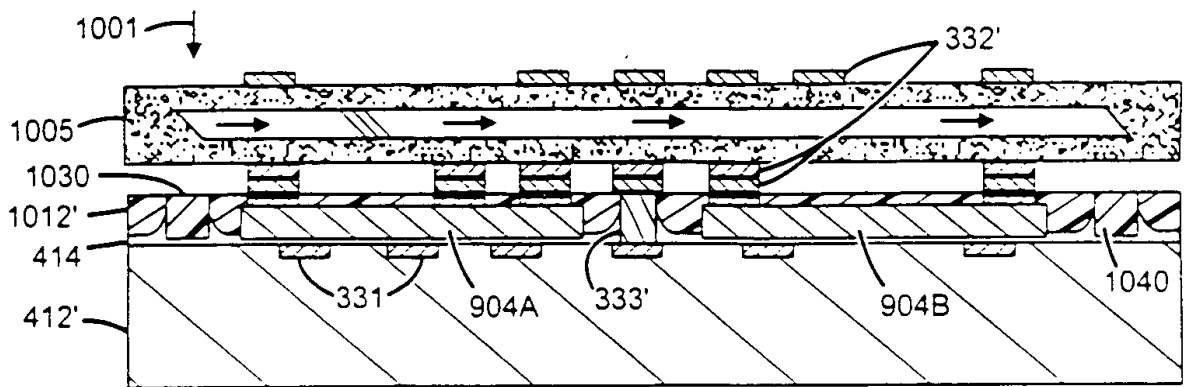


FIG._175

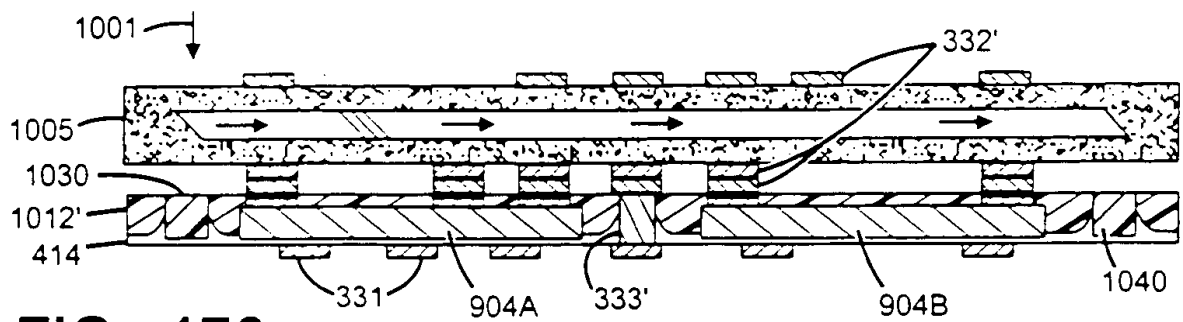


FIG._176

FIG. 174

1/XX

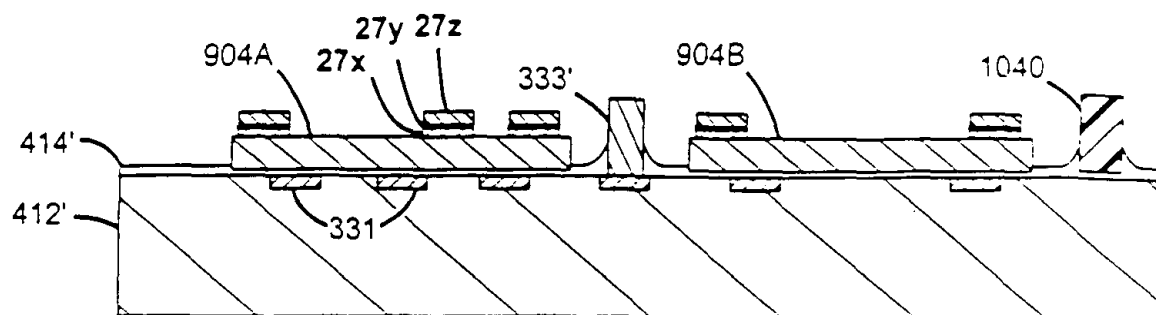


FIG._177

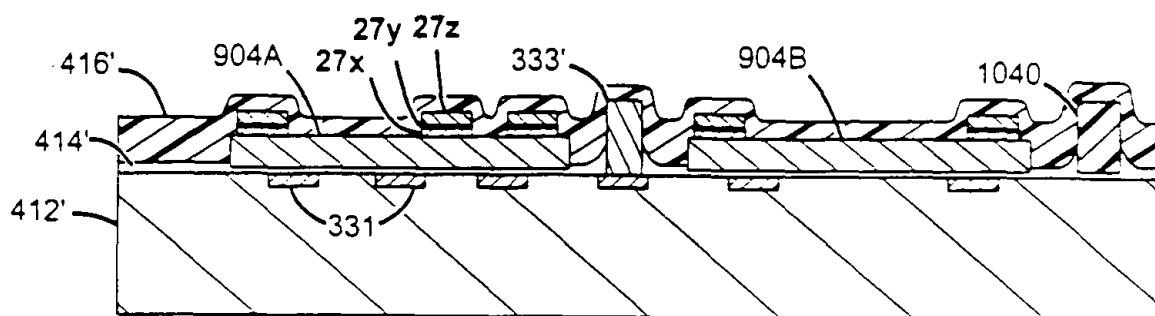


FIG._178

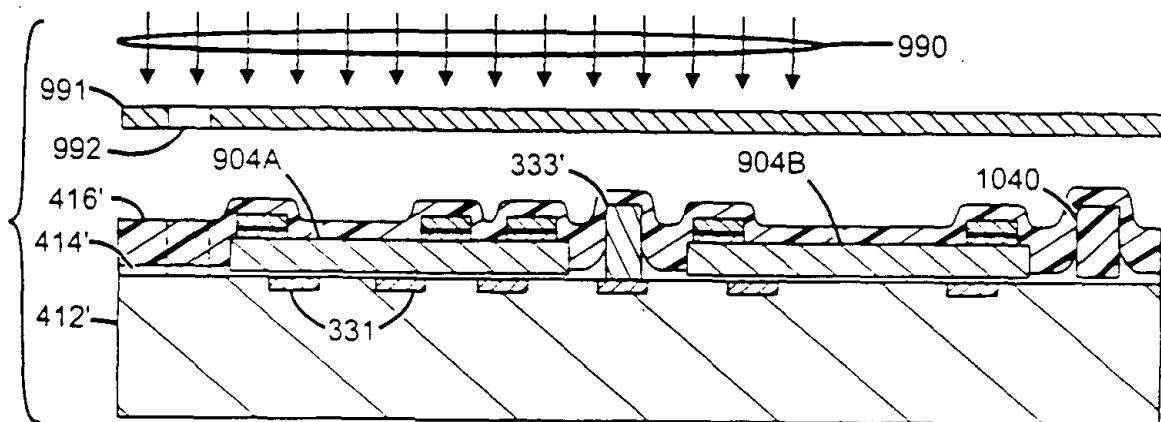


FIG._179

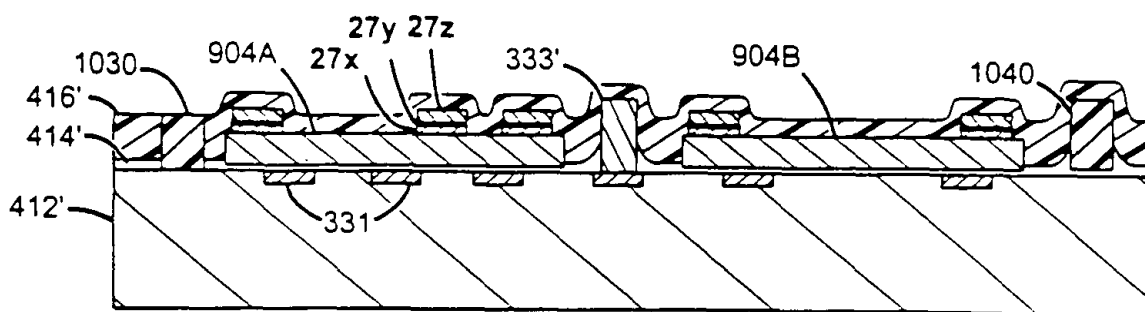


FIG._180

FIG. 177

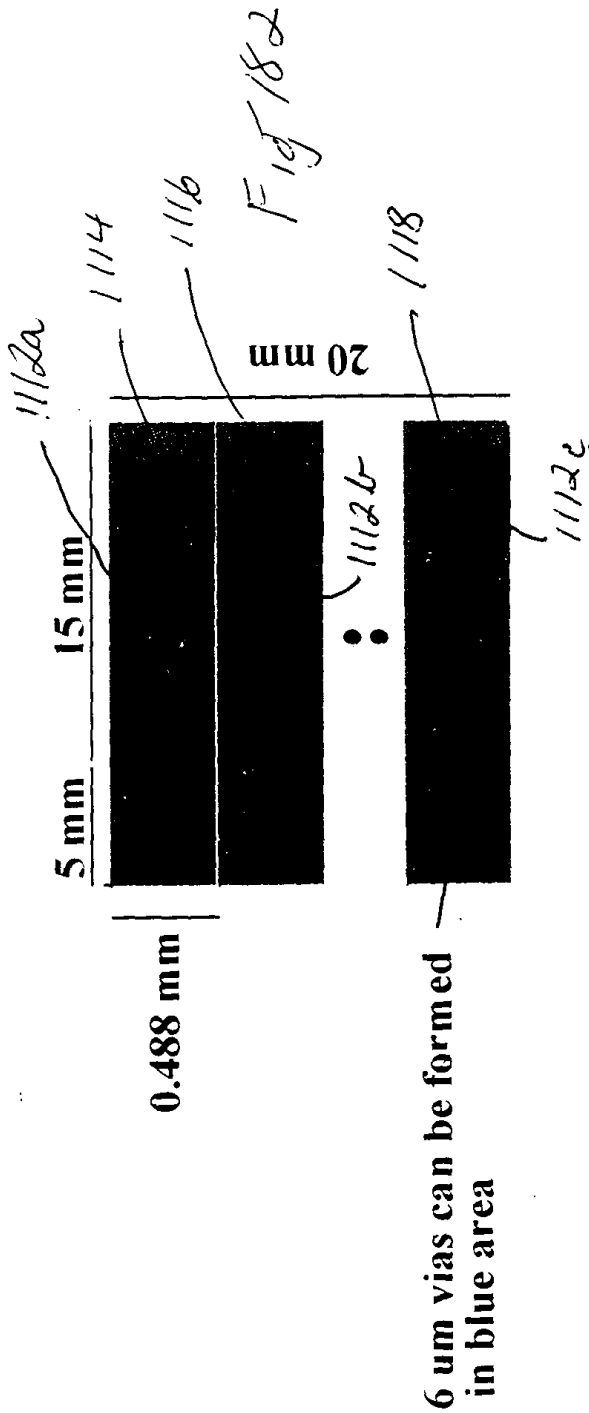
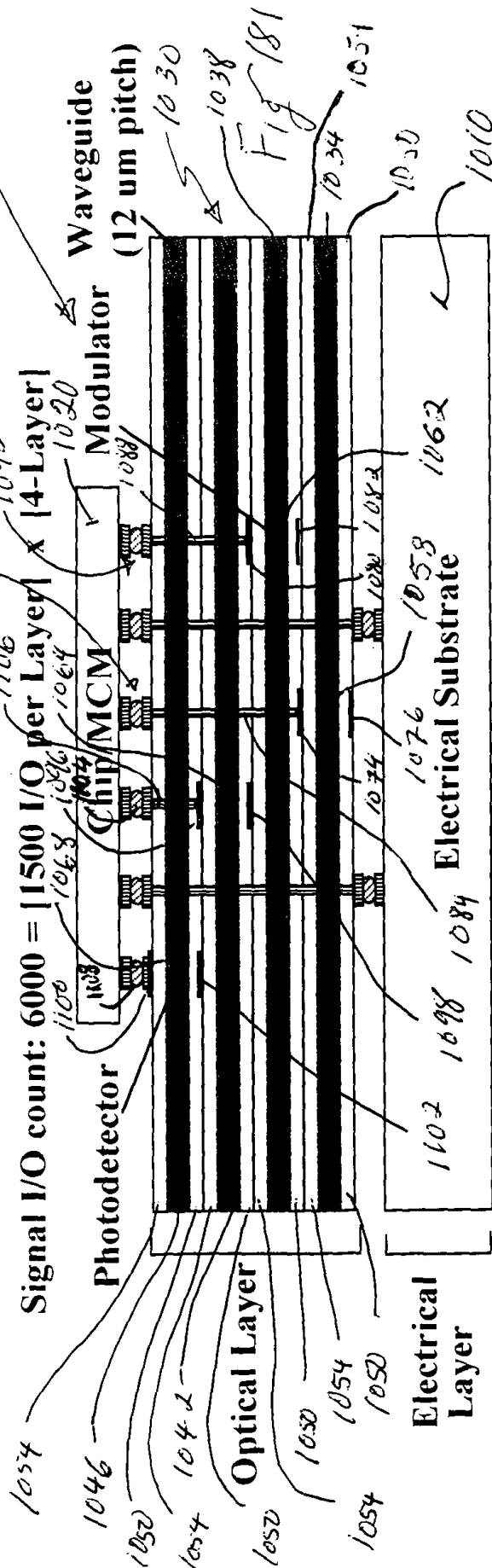
25916-180
98-23

FOOTNOTES

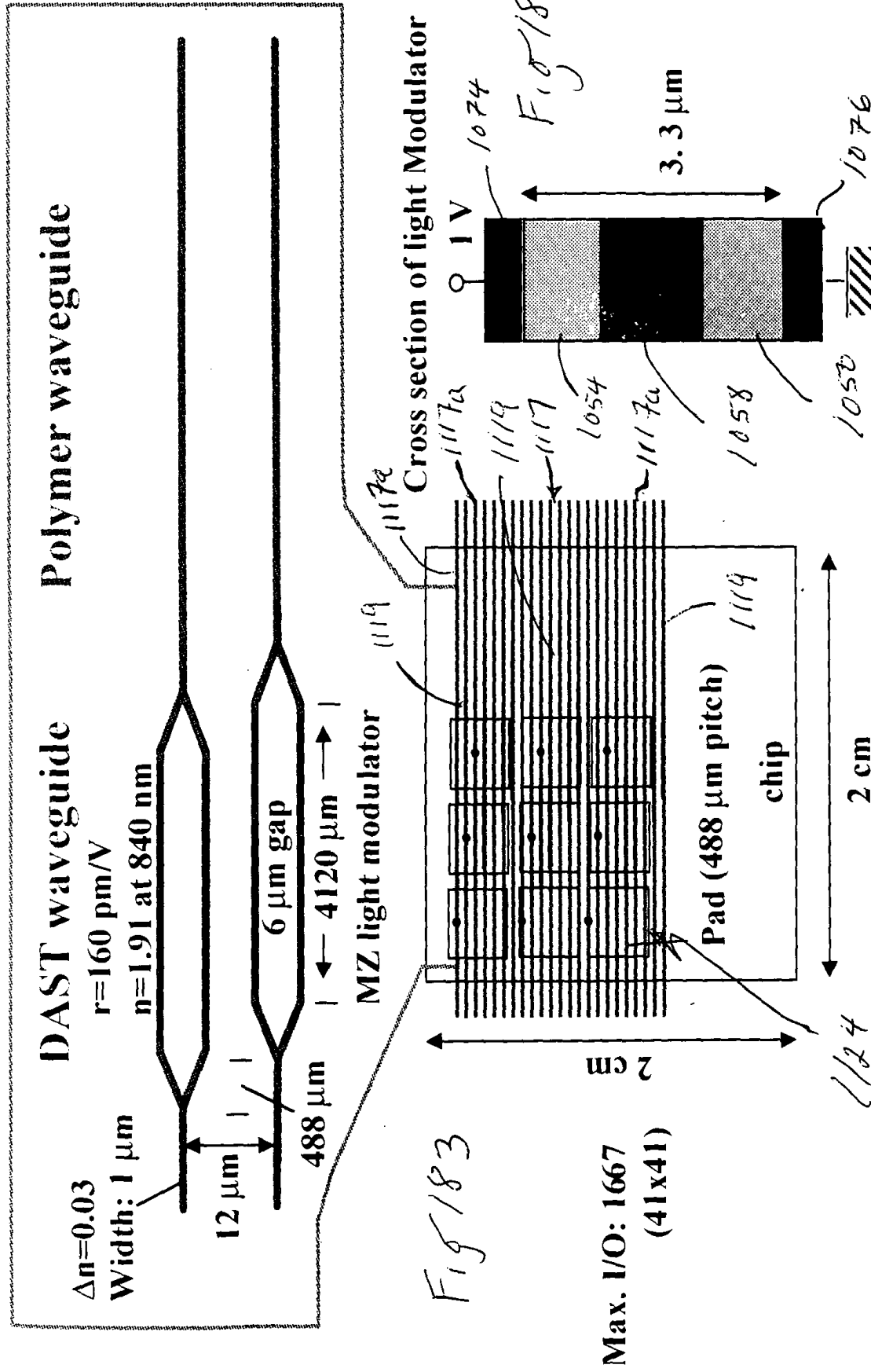
FUJITSU Computer Packaging Technologies, Inc.

FCPT

I/O Connection in OE Substrate (Planar Modulator)



I/O Connection in OE Substrate (Planar Modulator)



Max. I/O: 1667
(41x41)

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

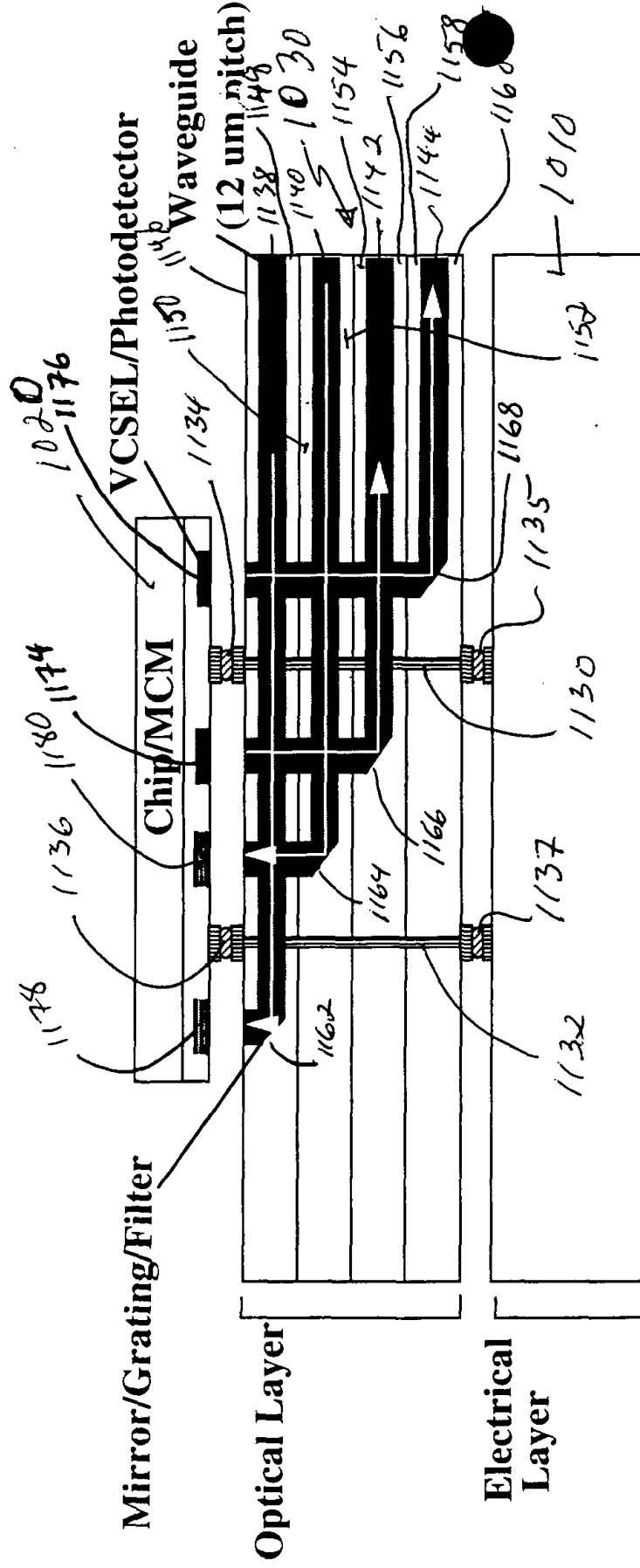


Fig 185

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

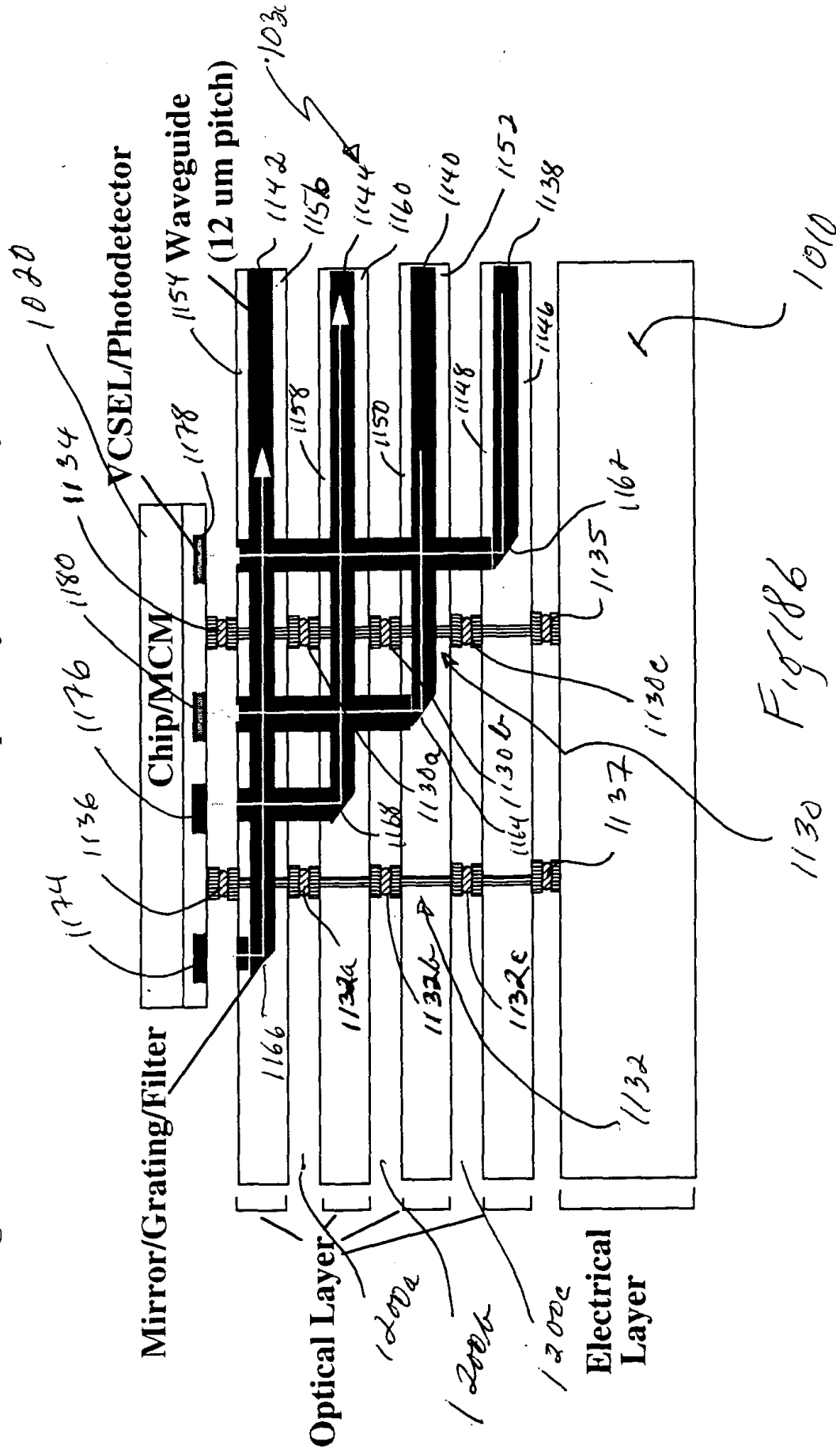


Fig.

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

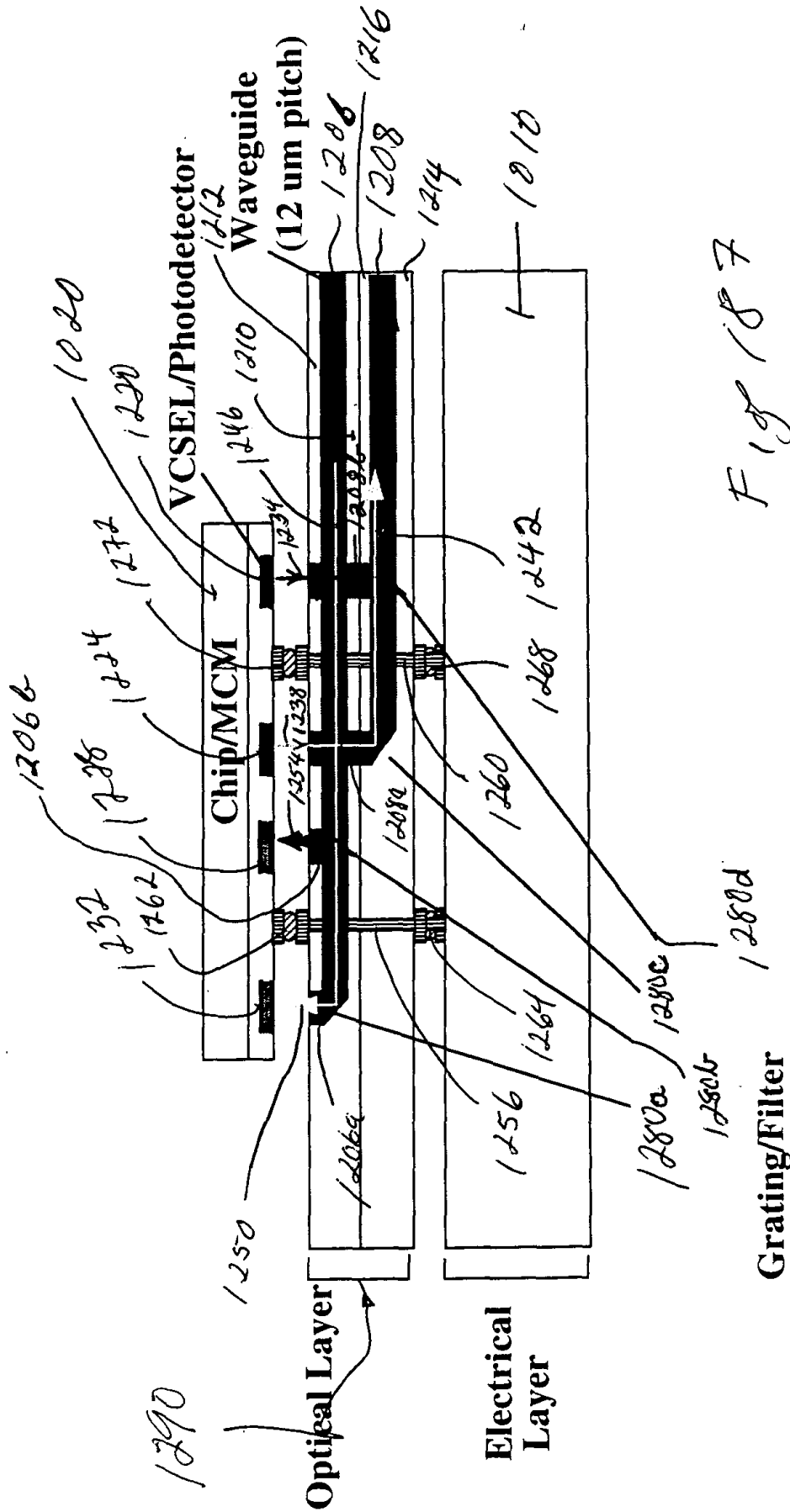


Fig 187

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

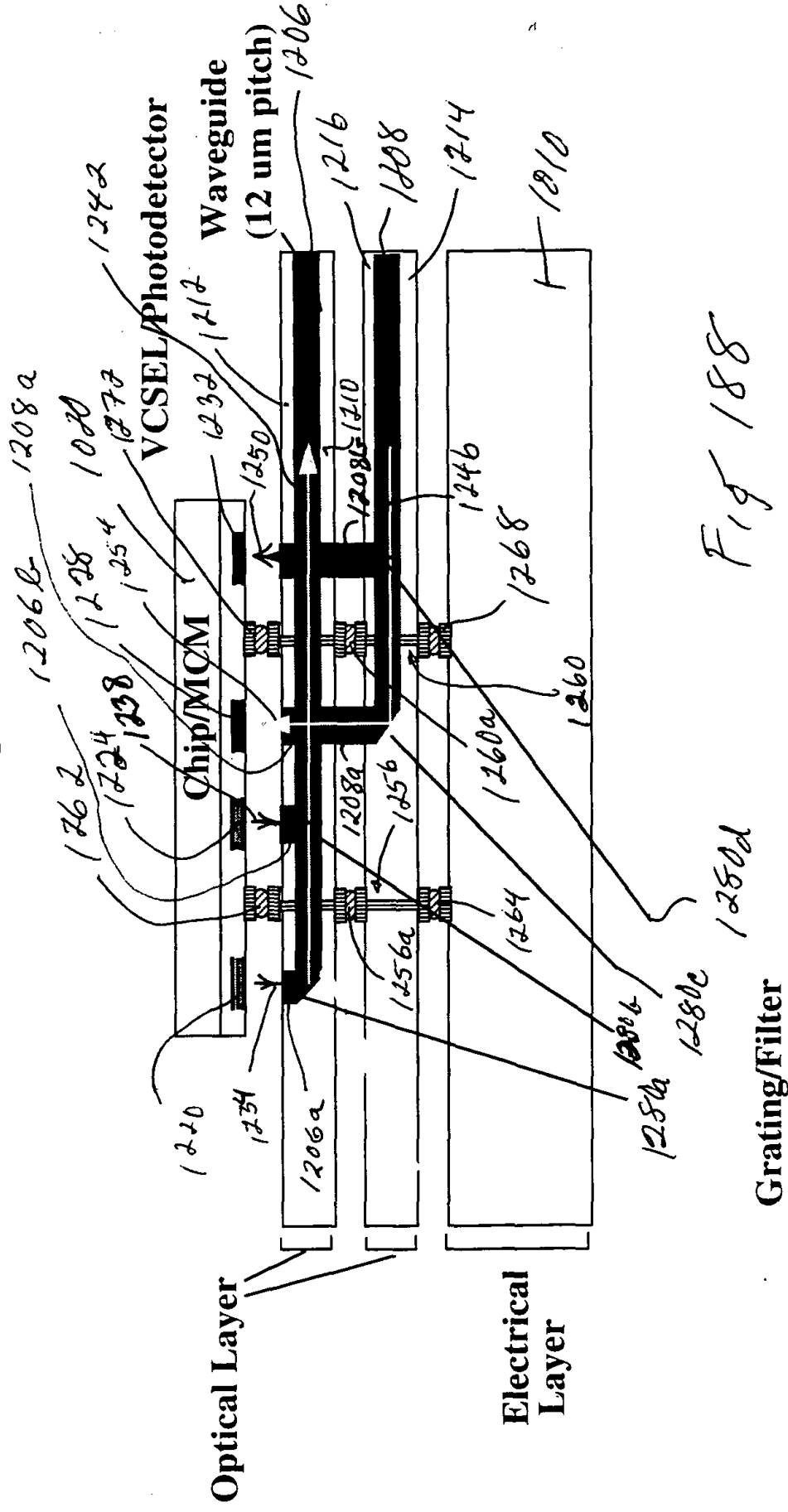


Fig 188

Grating/Filter

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

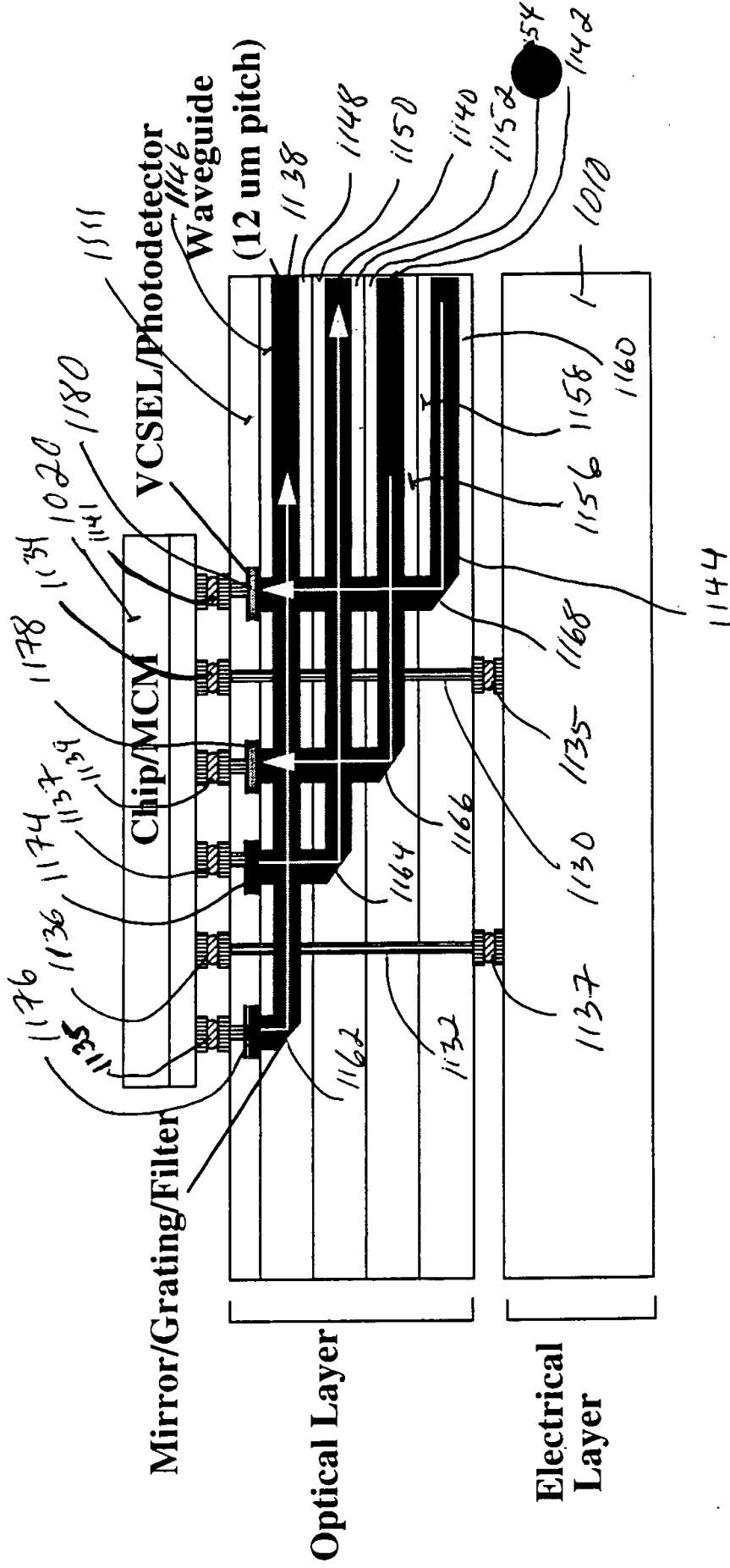


Fig 189

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

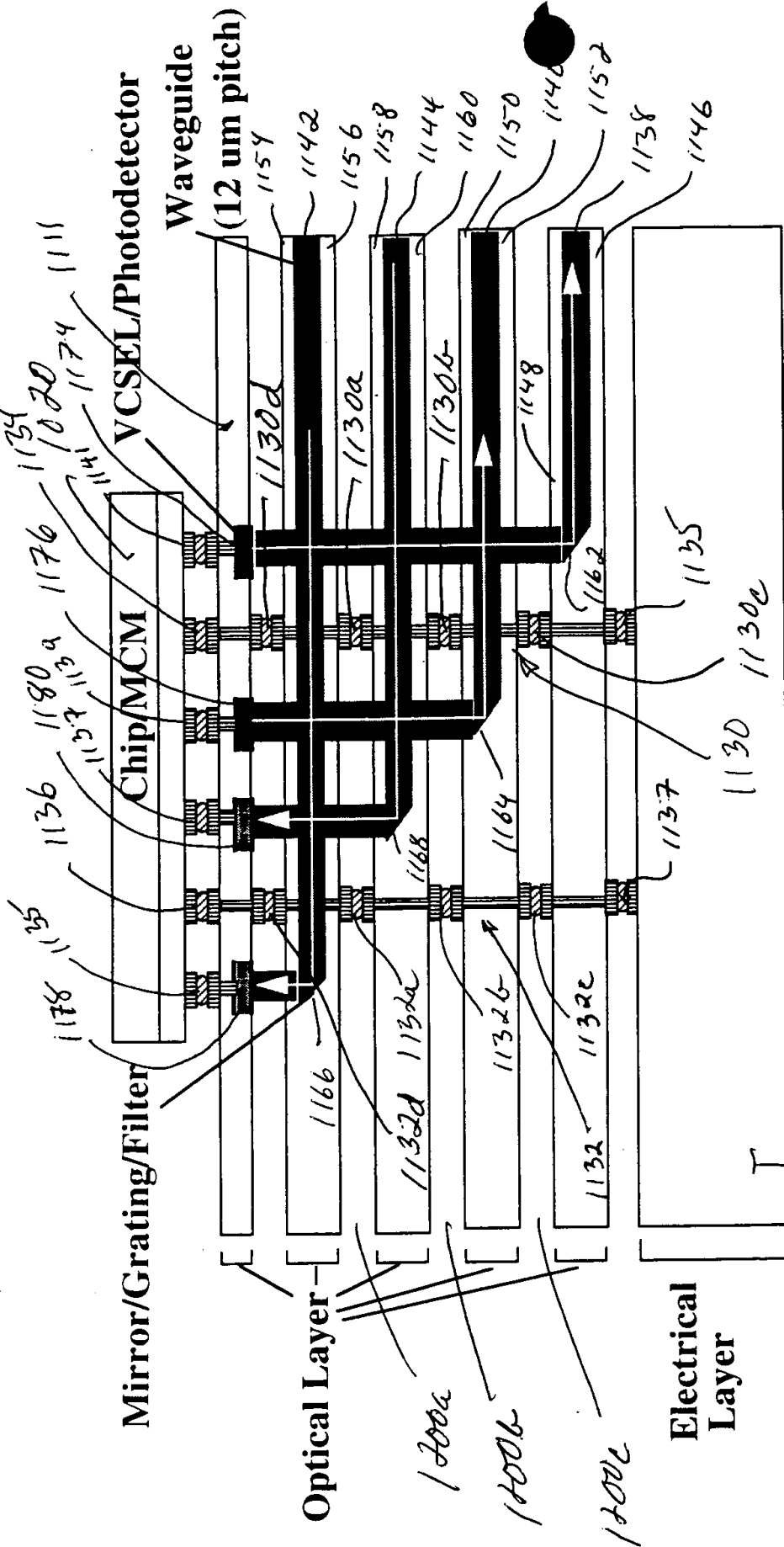


Fig 190

Fig. 9

I/O Connection in OE Substrate (Active OE Layer, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

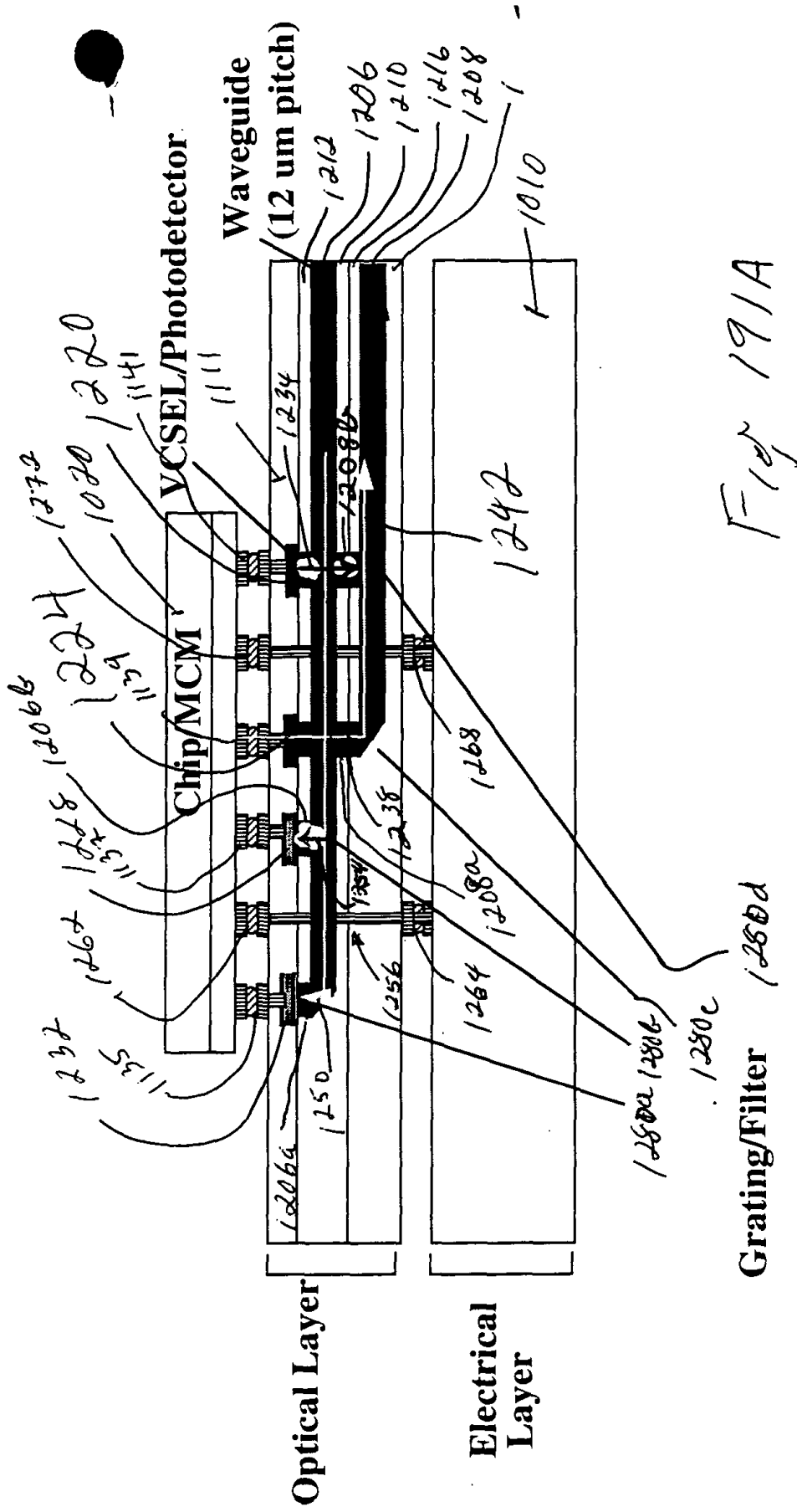


Fig. 10

I/O Connection in OE Substrate (Active OE Layer, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

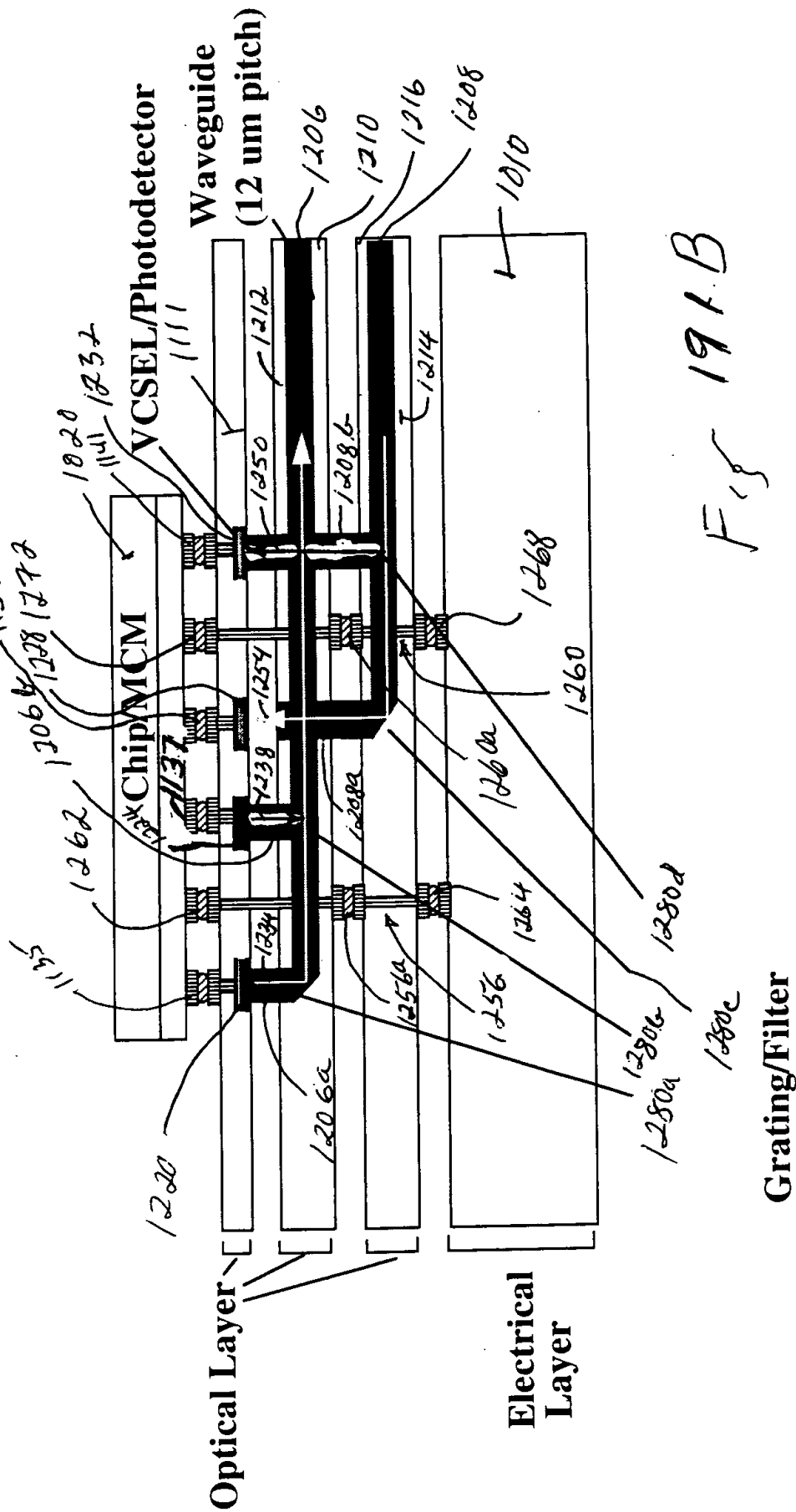
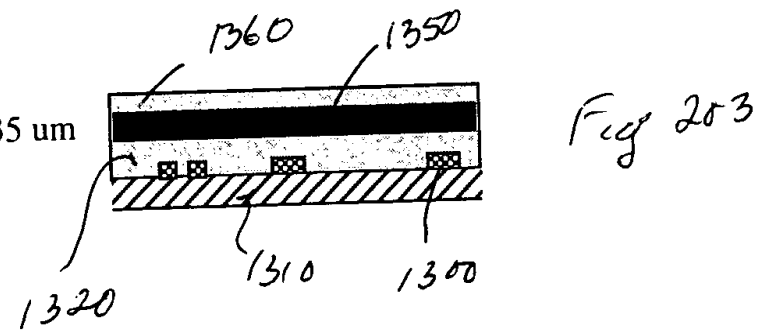
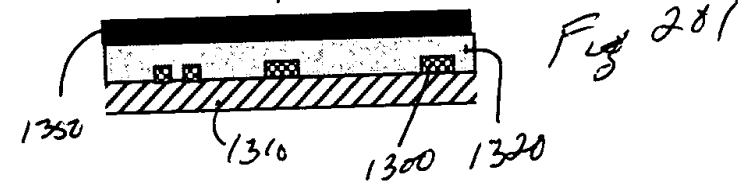
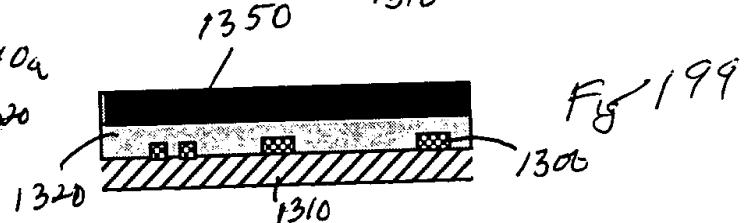
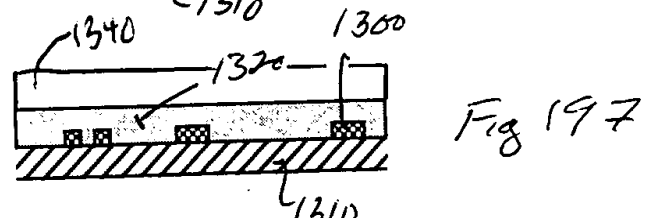
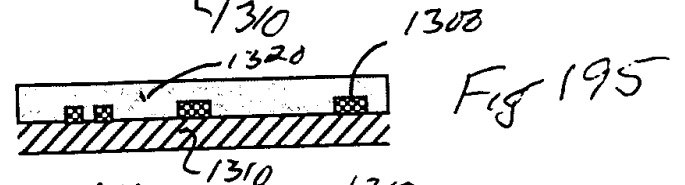
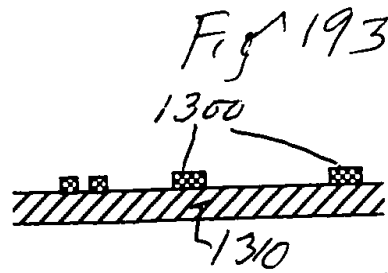
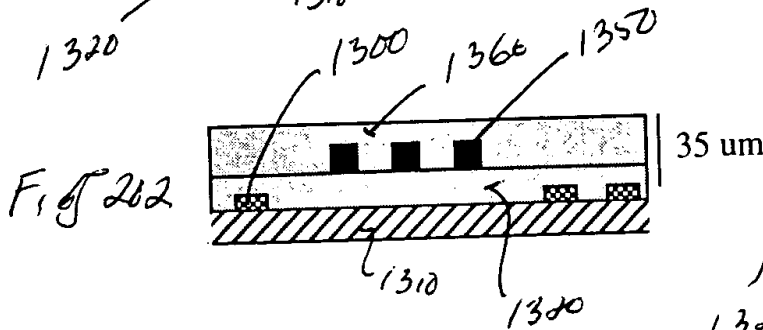
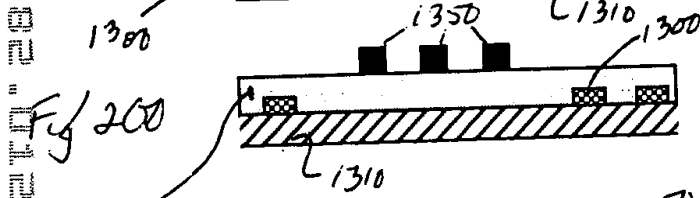
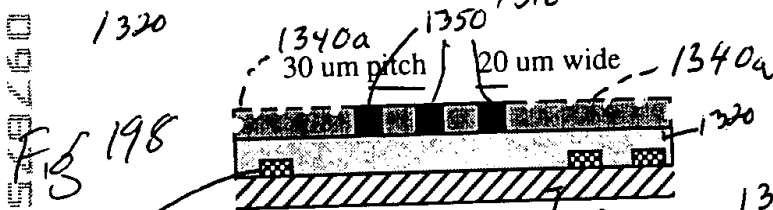
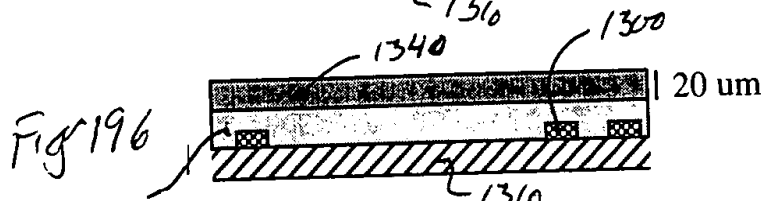
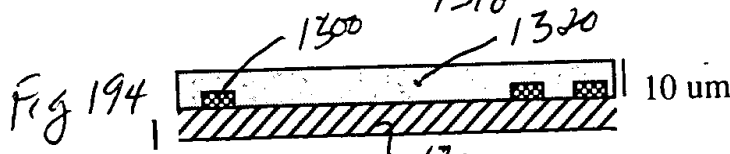
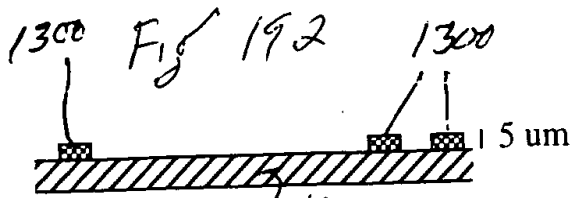
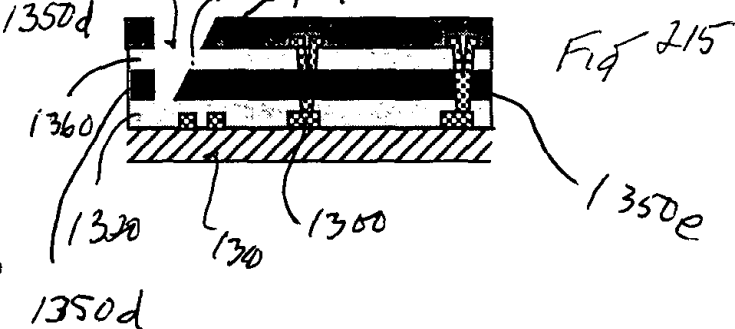
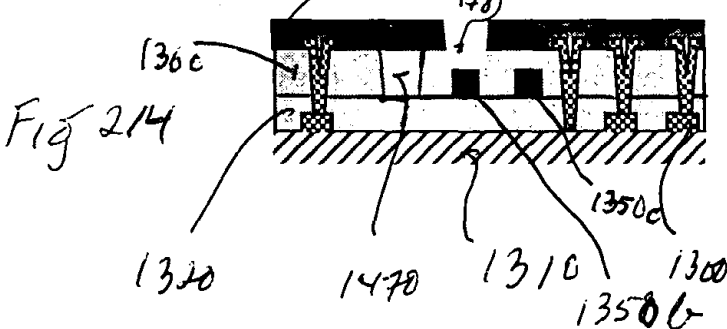
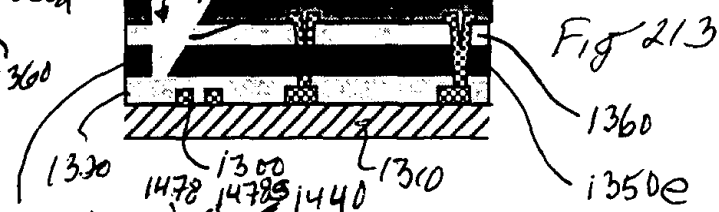
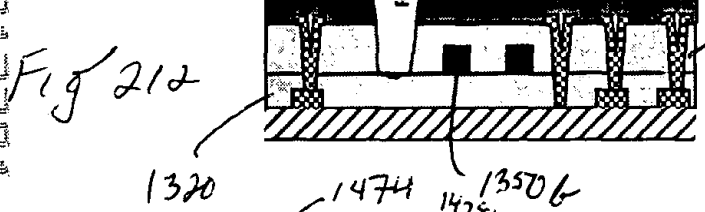
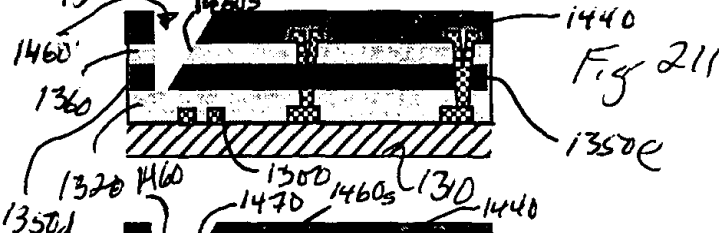
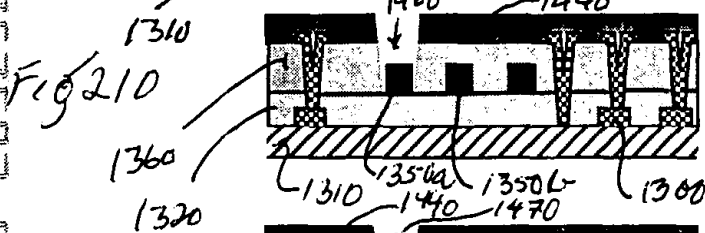
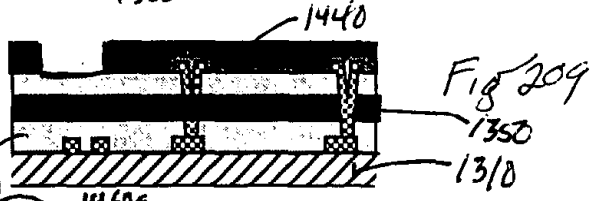
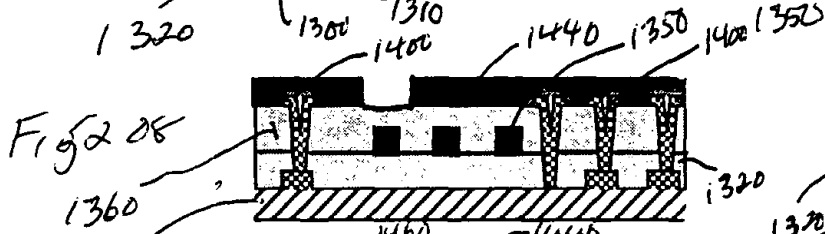
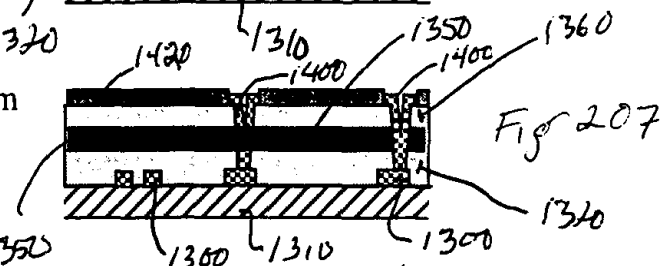
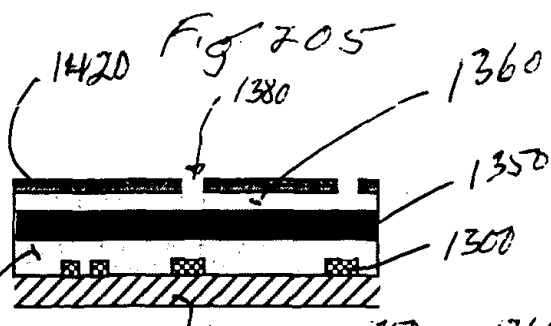
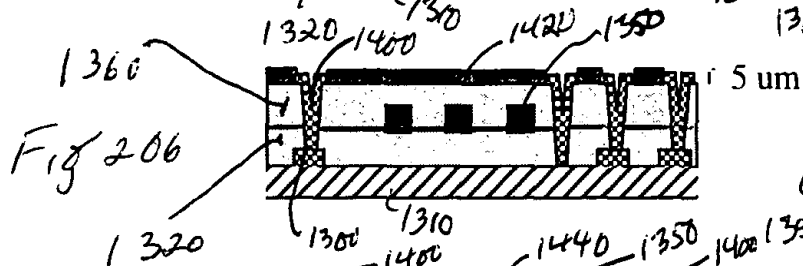
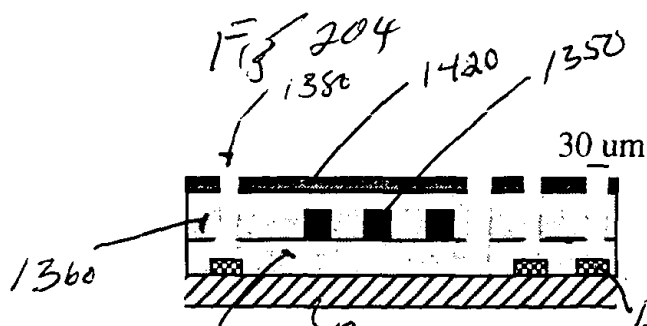


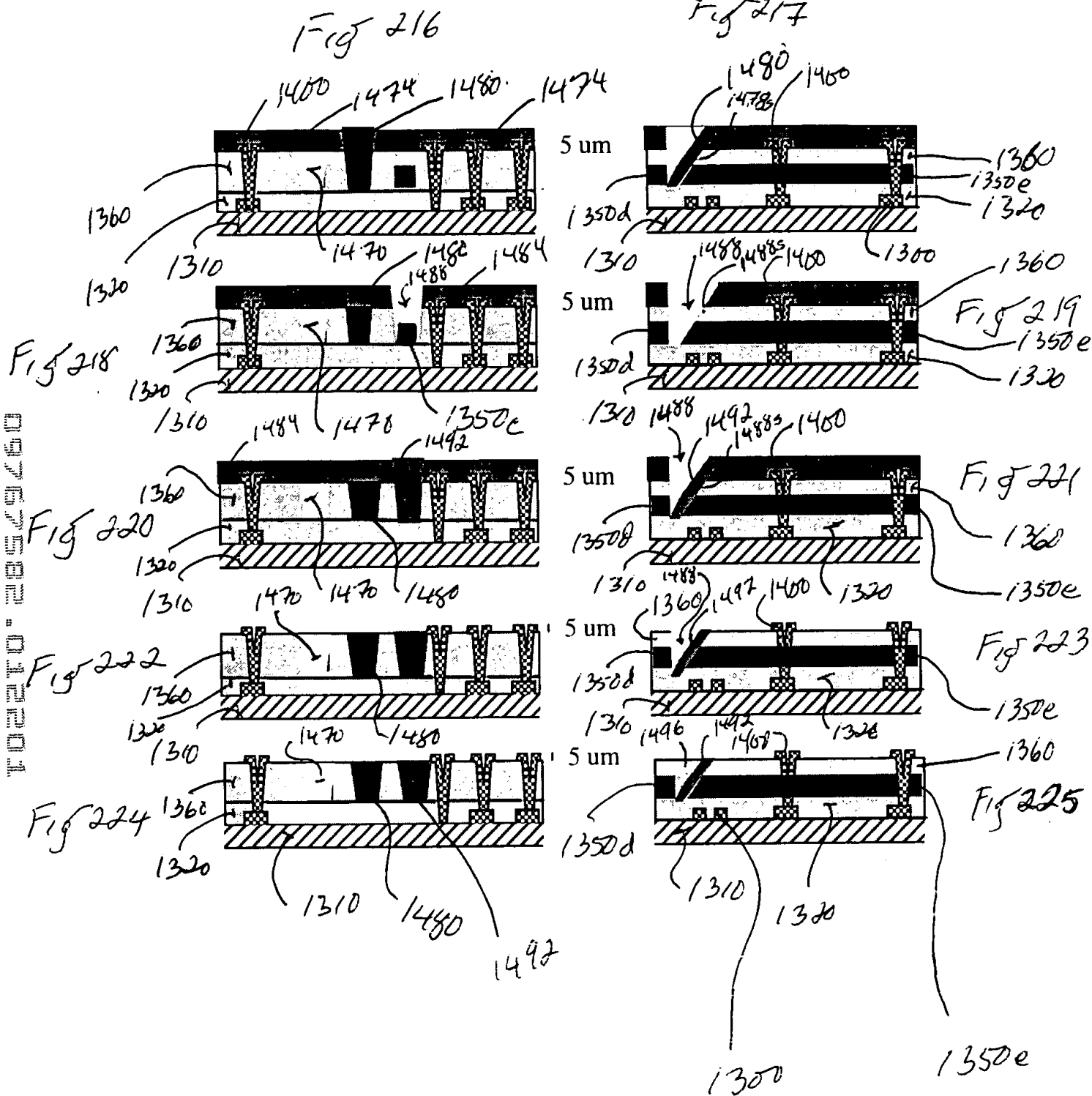
Fig. 11



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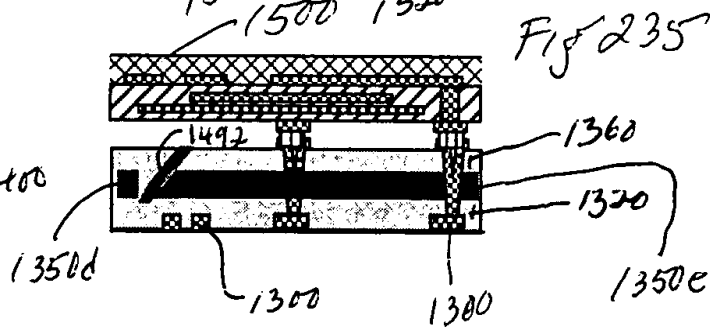
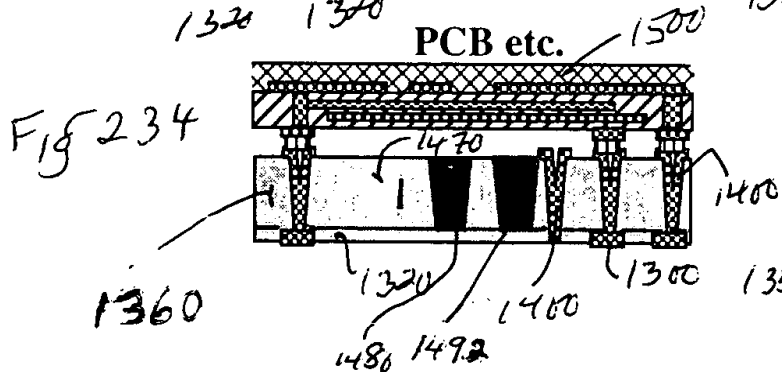
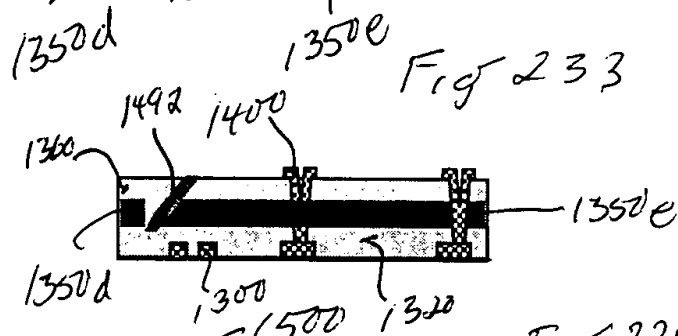
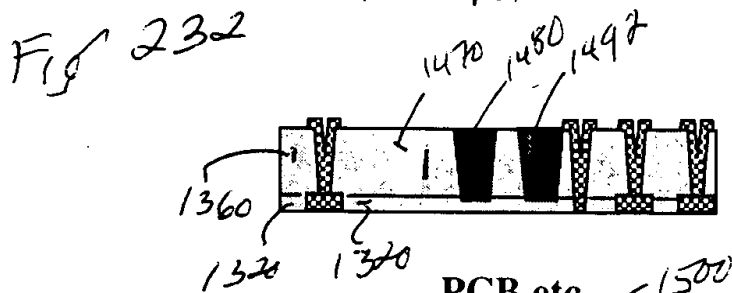
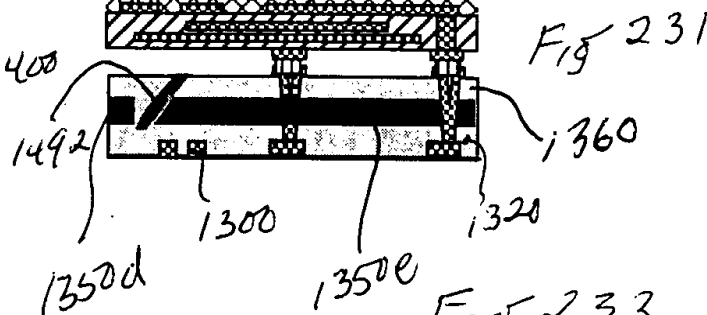
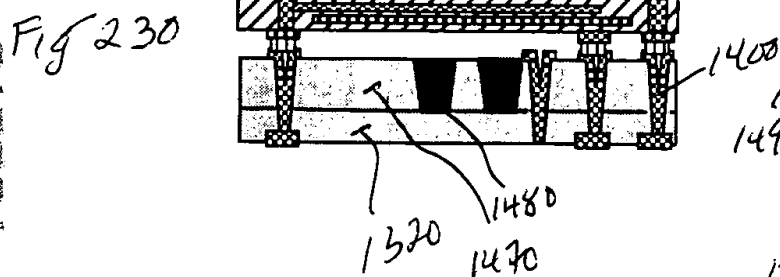
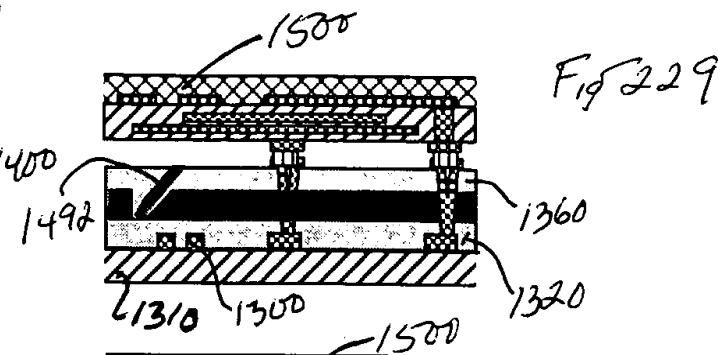
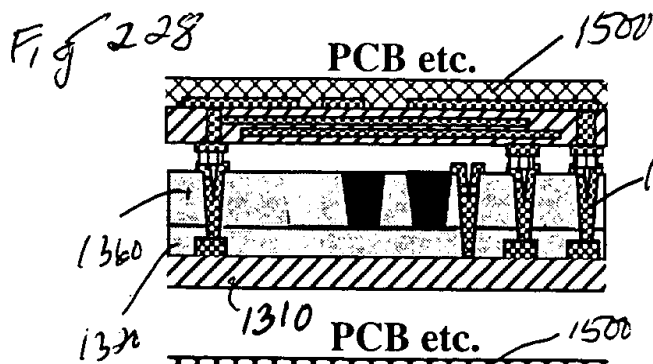
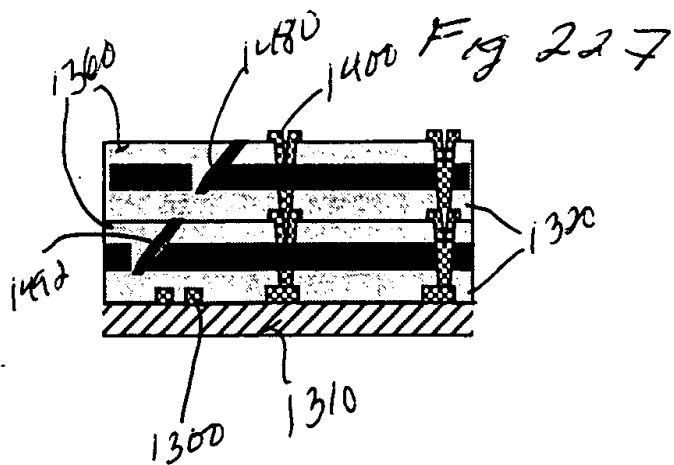
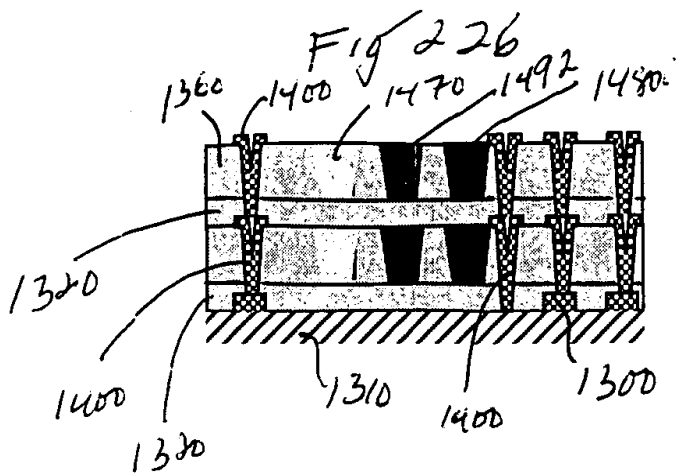


Fig 236

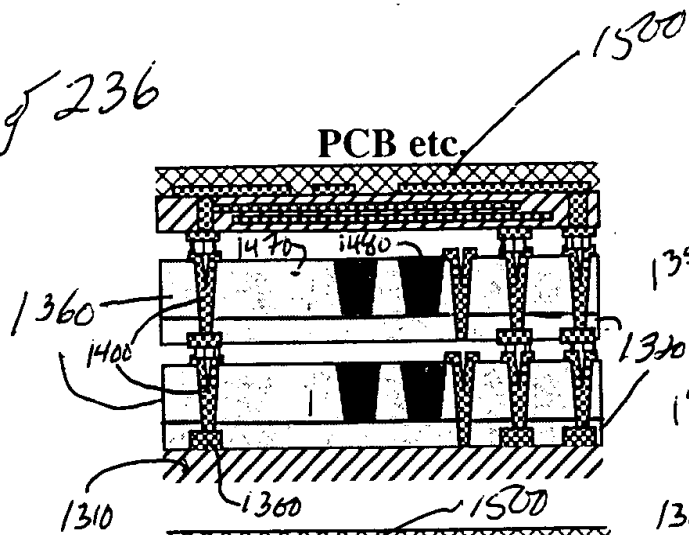


Fig 237

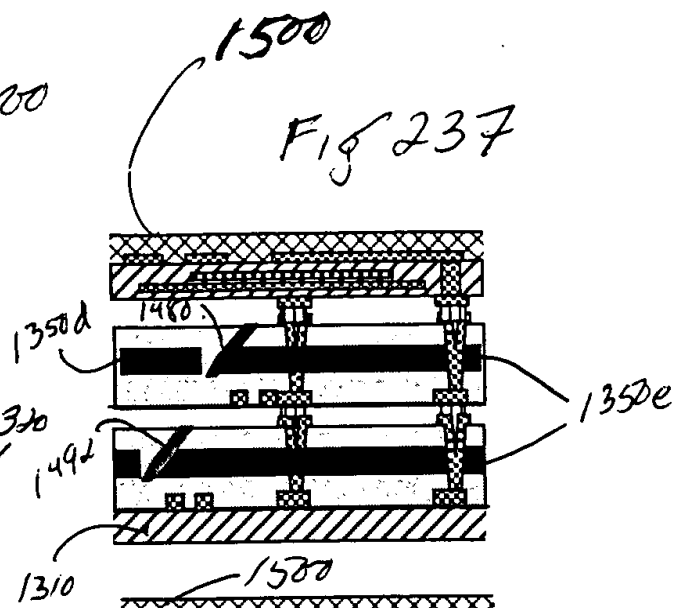


Fig 238

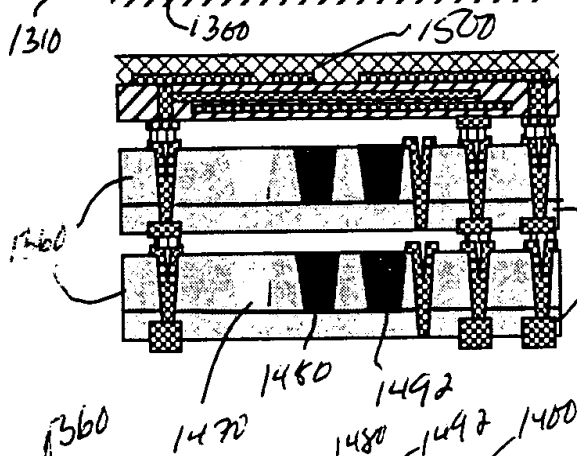


Fig 239

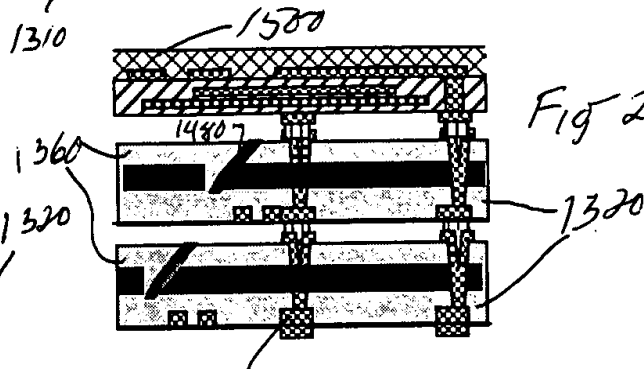


Fig 240

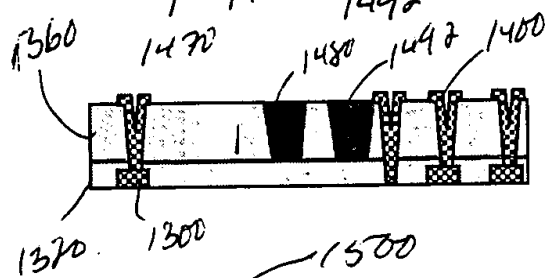


Fig 241

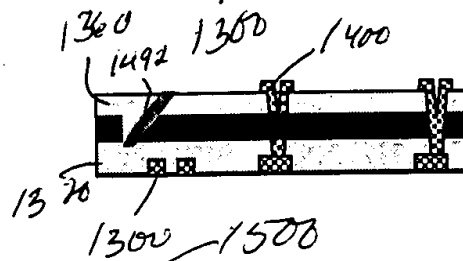


Fig 242

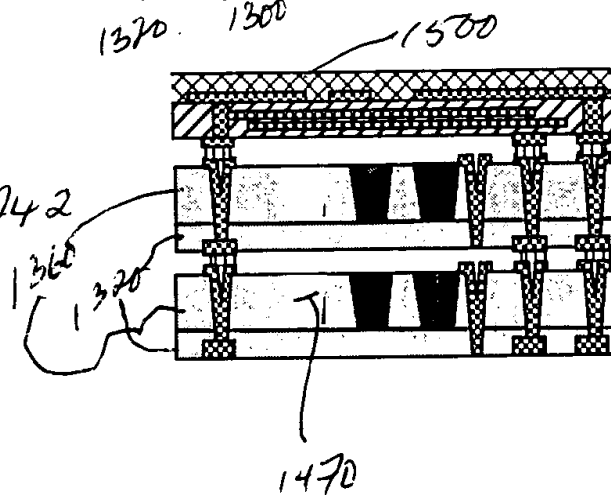


Fig 243

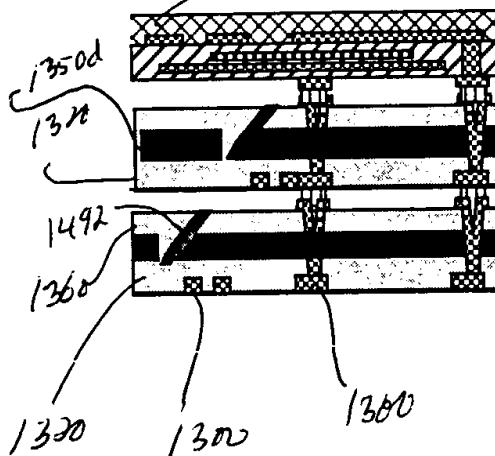


Fig 244

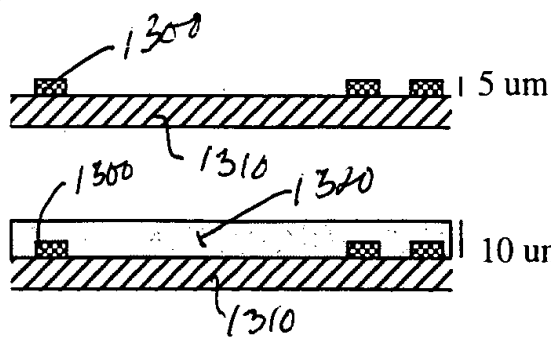


Fig 245

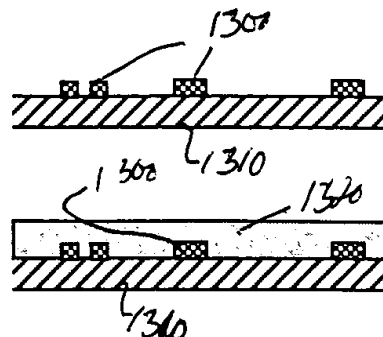


Fig 246

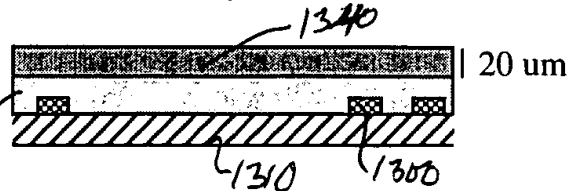


Fig 247

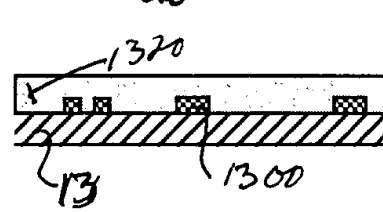


Fig 248

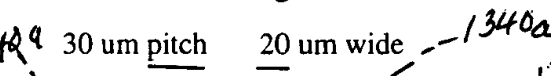


Fig 249

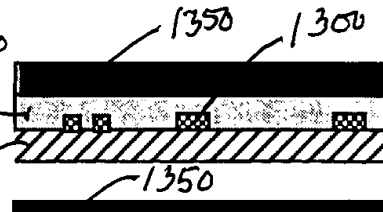


Fig 251

Fig 250

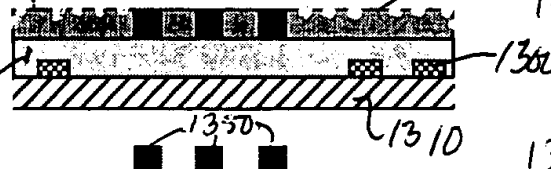


Fig 253

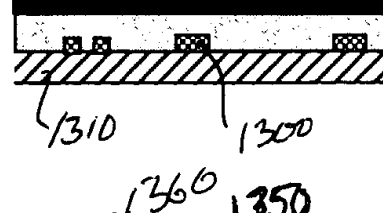


Fig 252

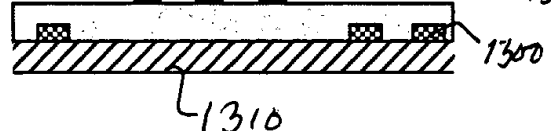


Fig 254

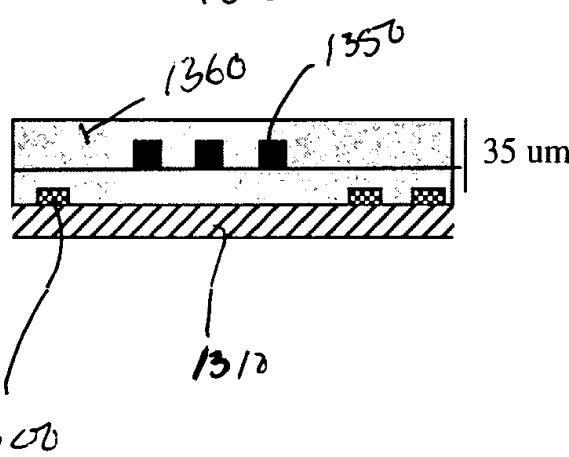
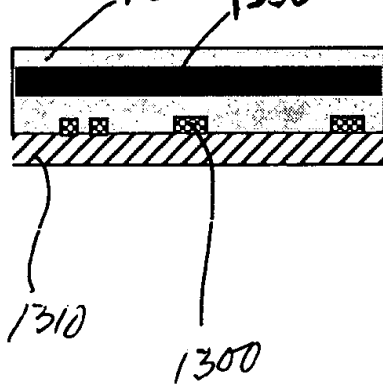


Fig 255



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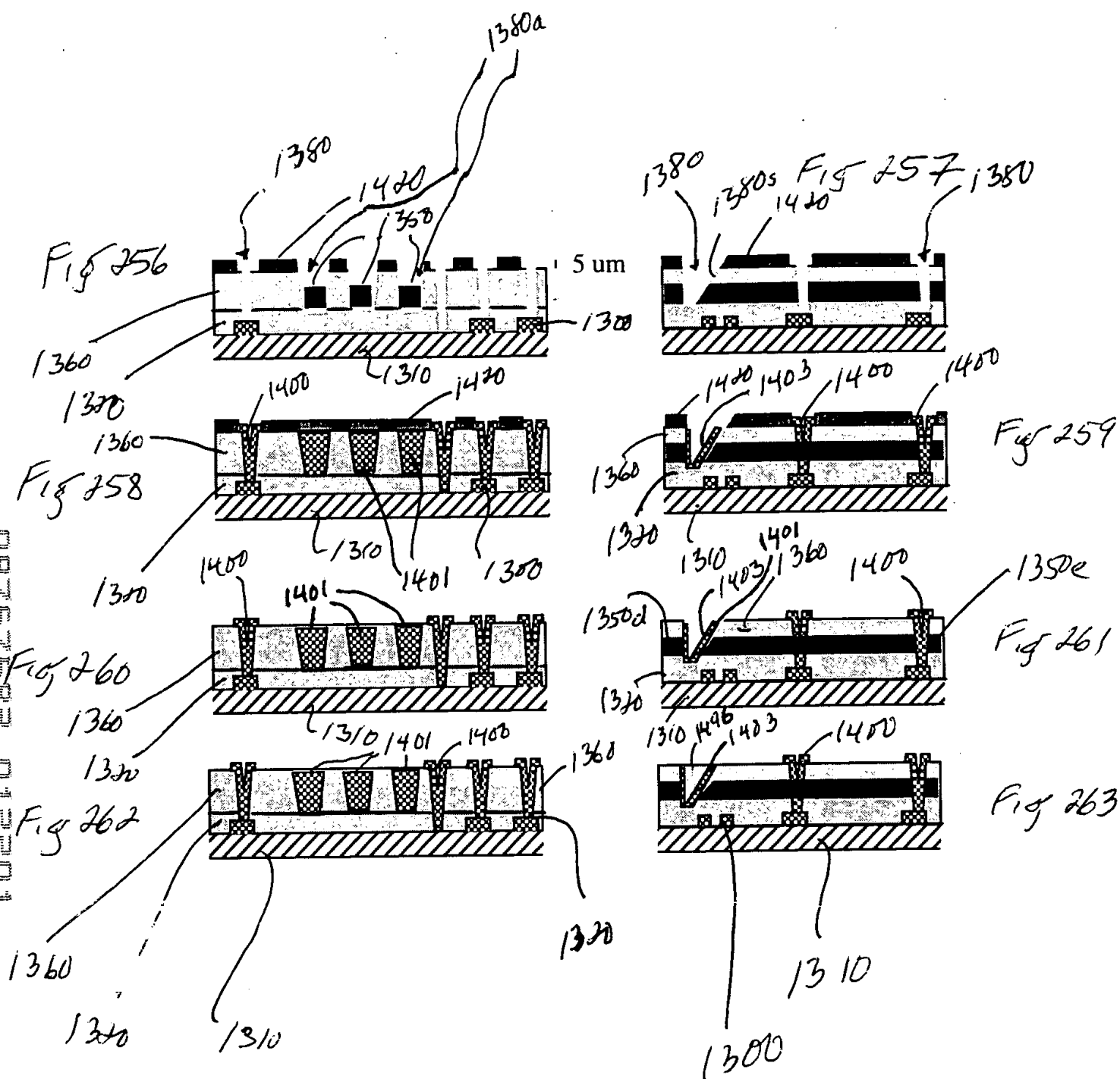
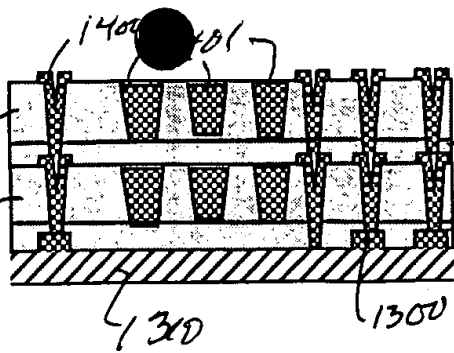


Fig 264

1360



1320

1360

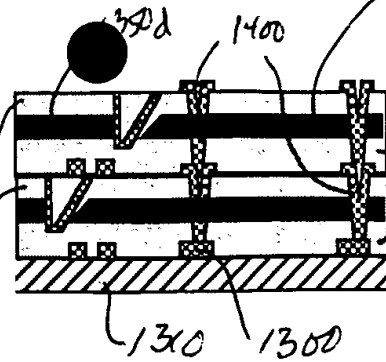


Fig 265

1320

1300

1350e

Fig 266

1300

5 um



1320

1300

Fig 267

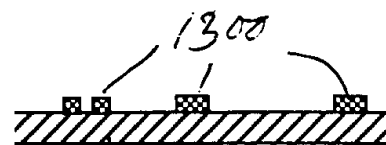


Fig 269

Fig 268

10 um



Fig 270

20 um

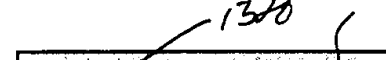


Fig 271

Fig 272

30 um pitch

20 um wide

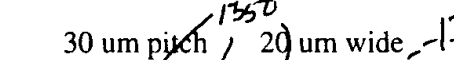


Fig 273

Fig 274



Fig 275

Fig 276

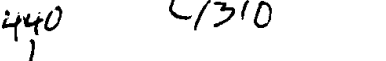
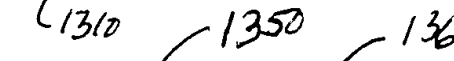


Fig 277

1320

1310

1350

1310

1300

1320

09767582.012201

09767582.012201

Fig 278

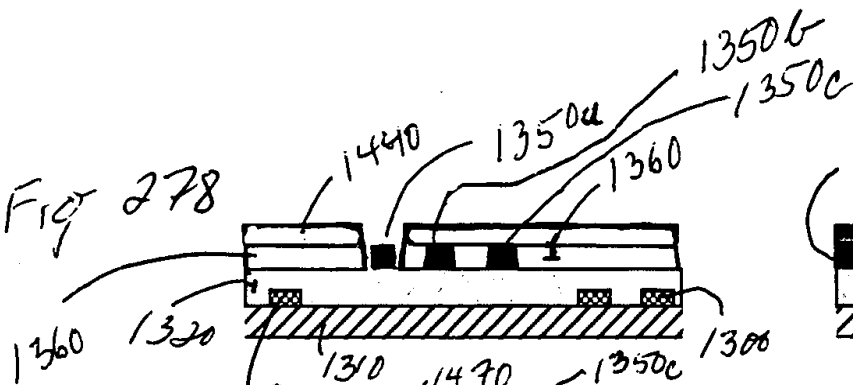


Fig 280

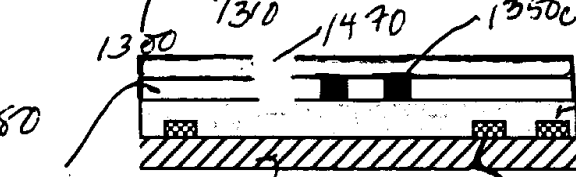


Fig 282

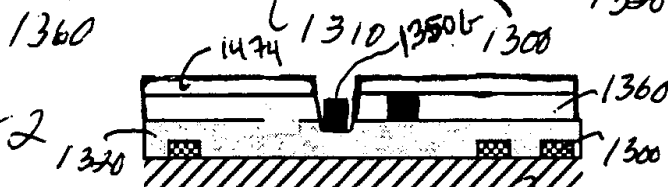


Fig 284

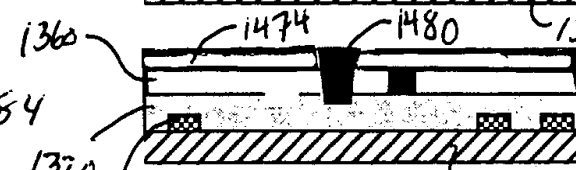


Fig 286

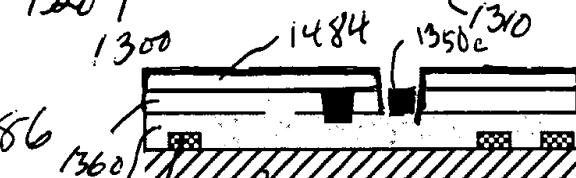


Fig 288

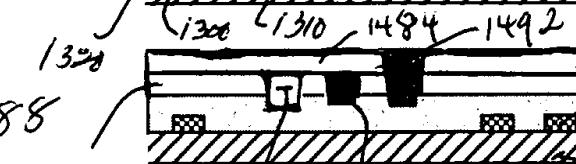


Fig 290

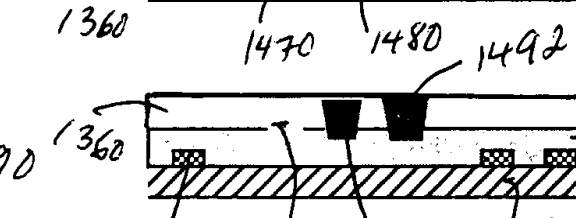


Fig 279

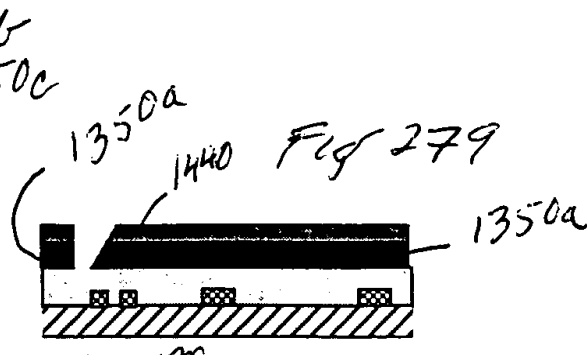


Fig 281

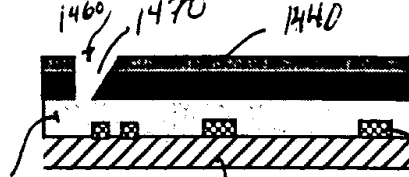


Fig 283

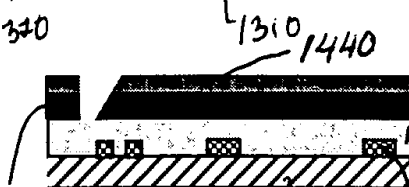


Fig 285

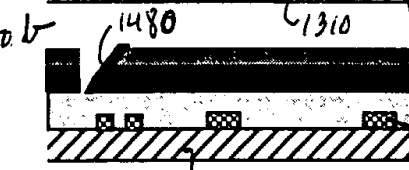


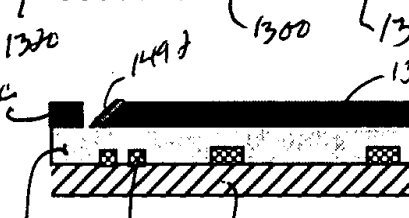
Fig 287

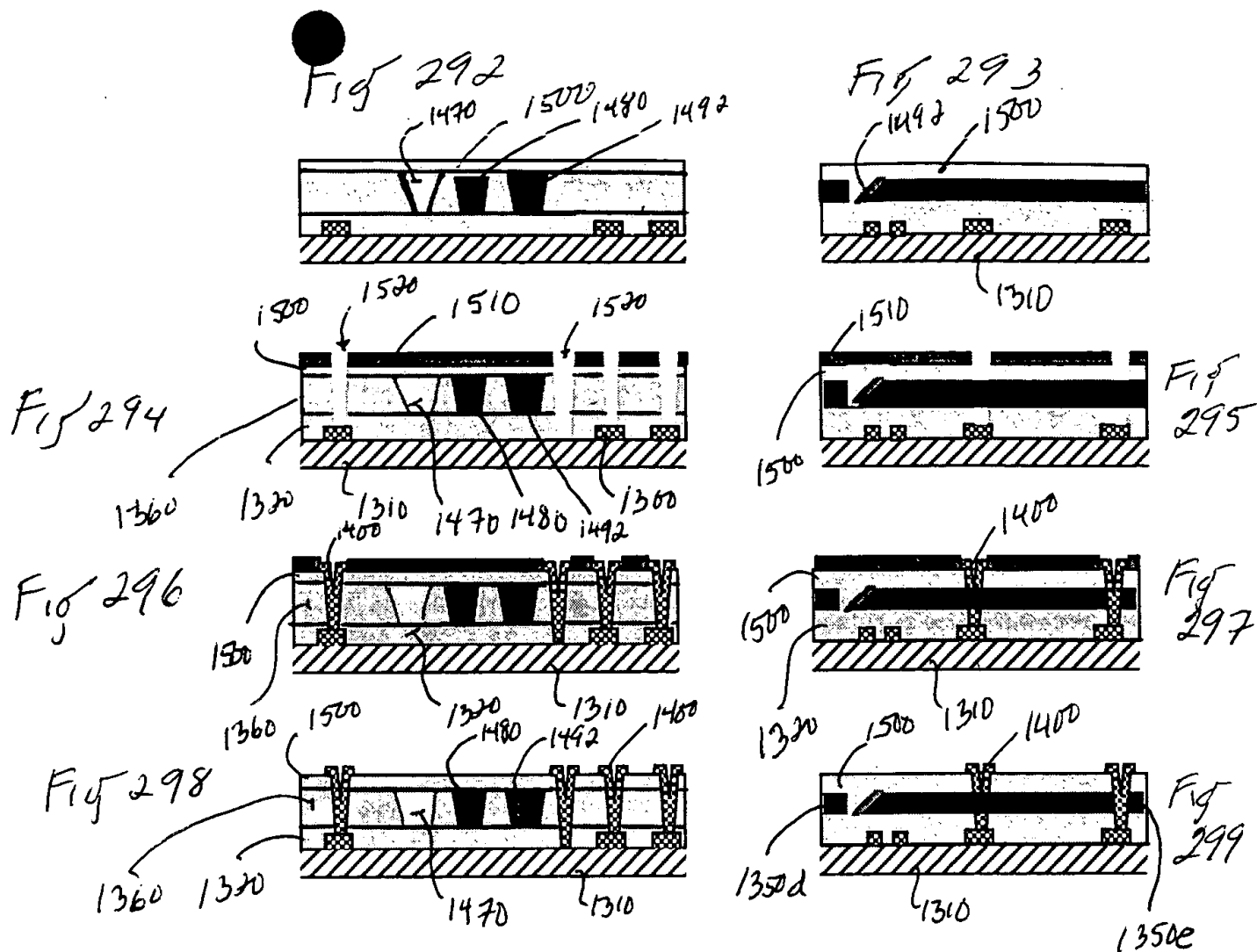


Fig 289



Fig 291





In the case of multi layer (a1-a16) process is repeated on the (a16).
 -it is also possible to repeat (a3-a16) or (a1, a3-a16)

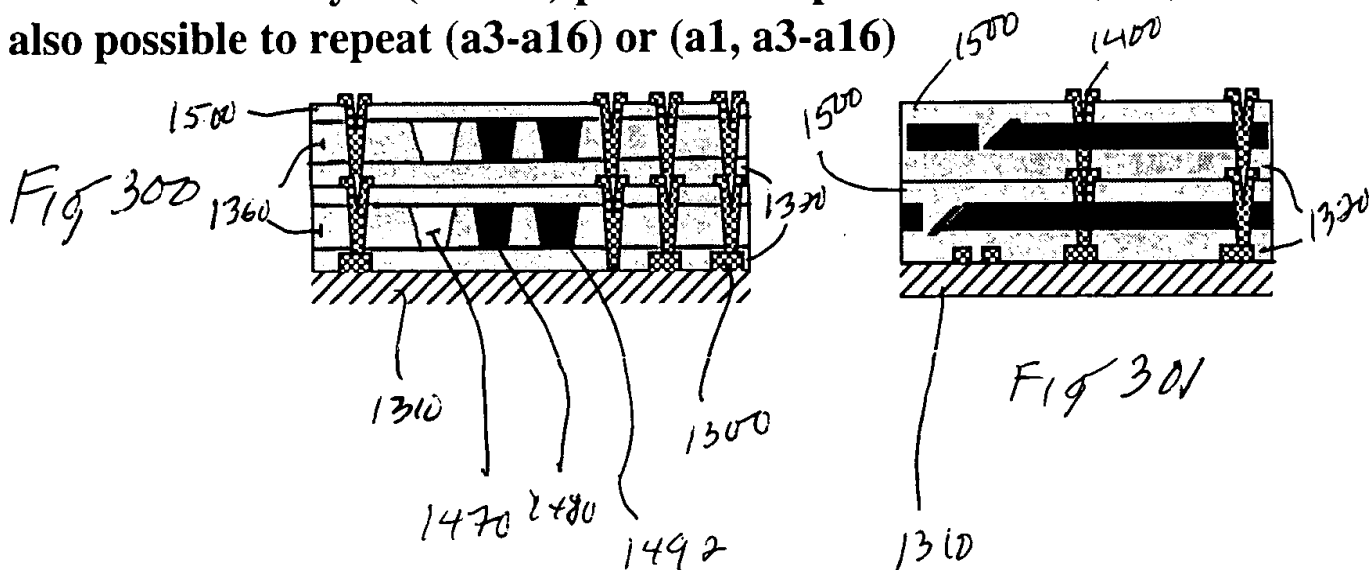


Fig 302

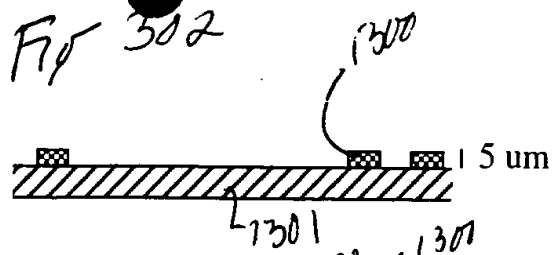


Fig 303

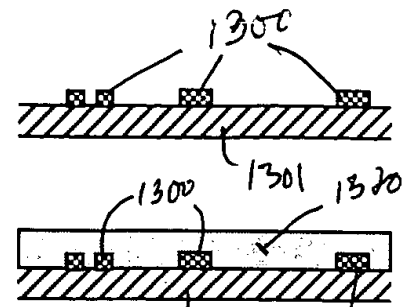


Fig 304

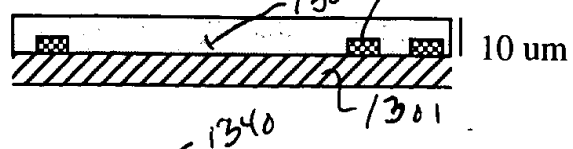


Fig 305

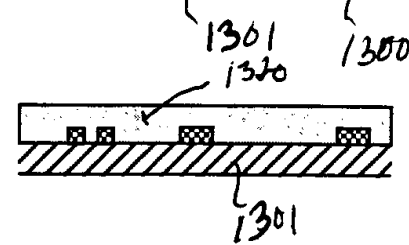


Fig 306

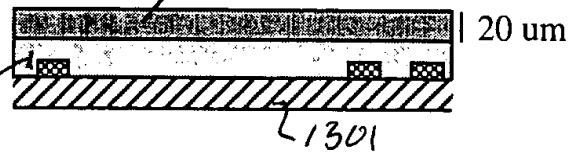


Fig 307

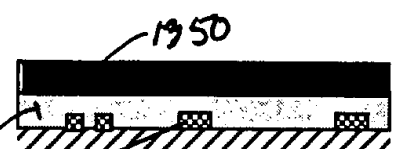


Fig 308

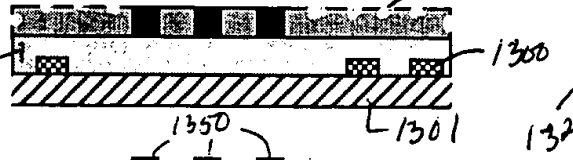


Fig 309



Fig 310

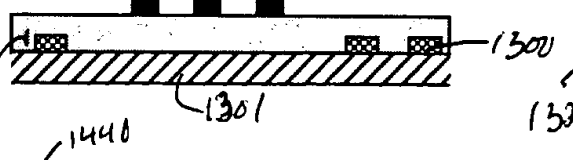


Fig 311

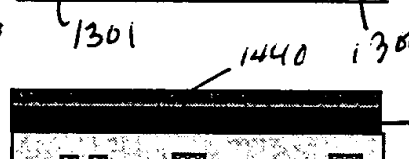


Fig 312

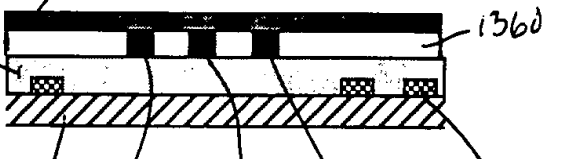
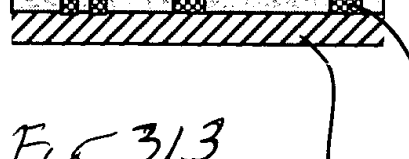
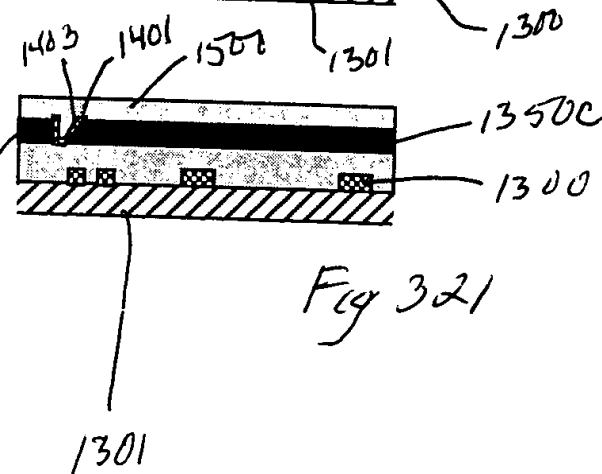
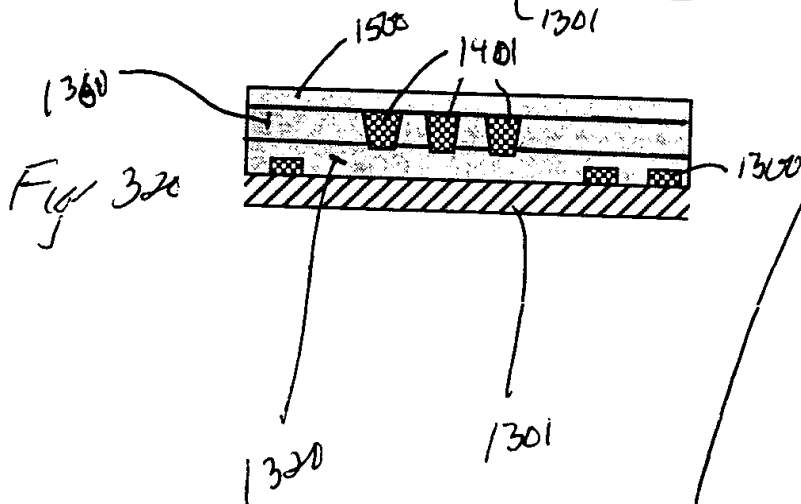
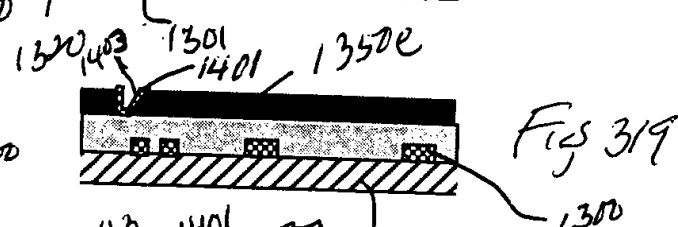
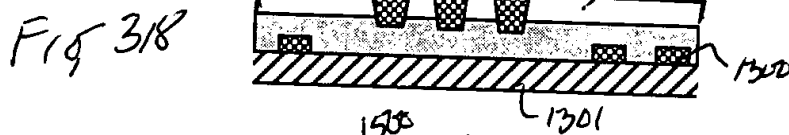
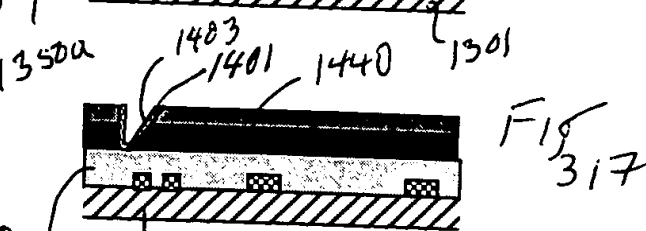
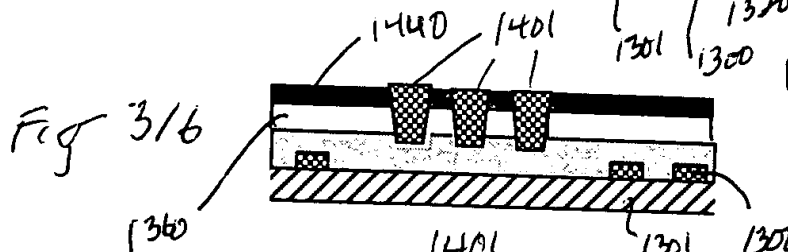
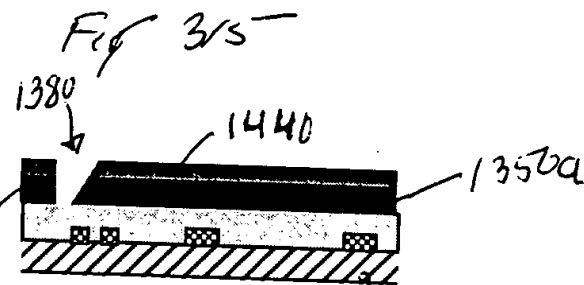
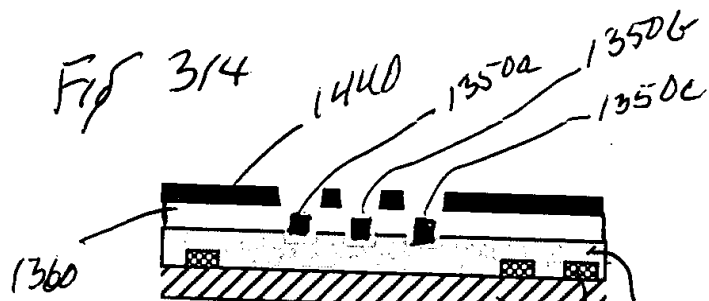


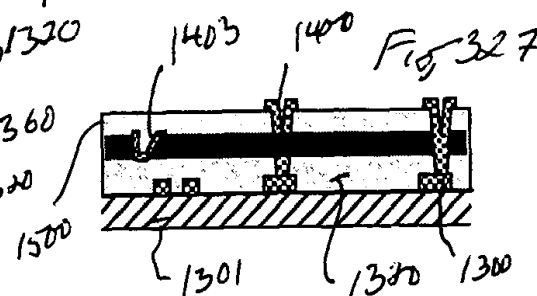
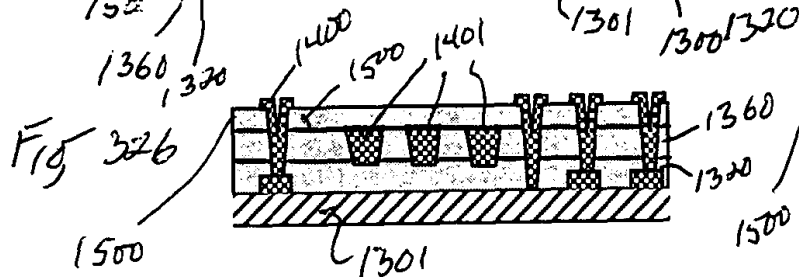
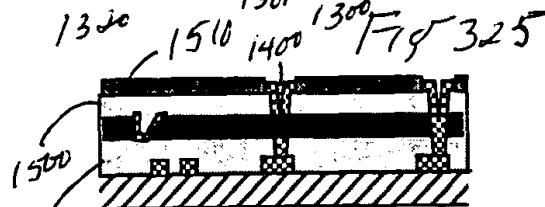
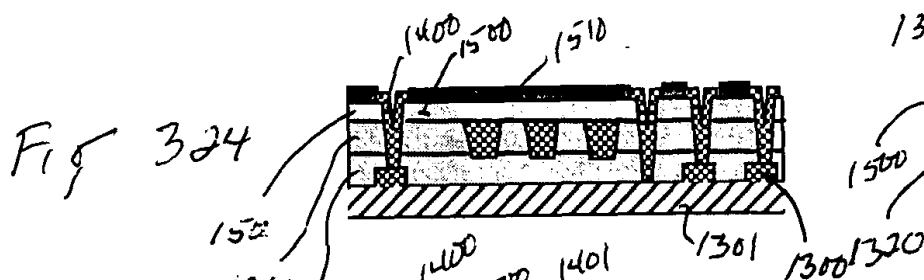
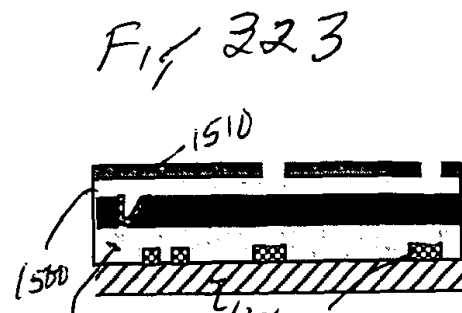
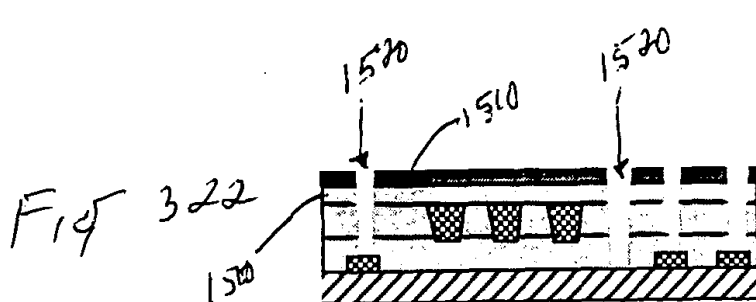
Fig 313



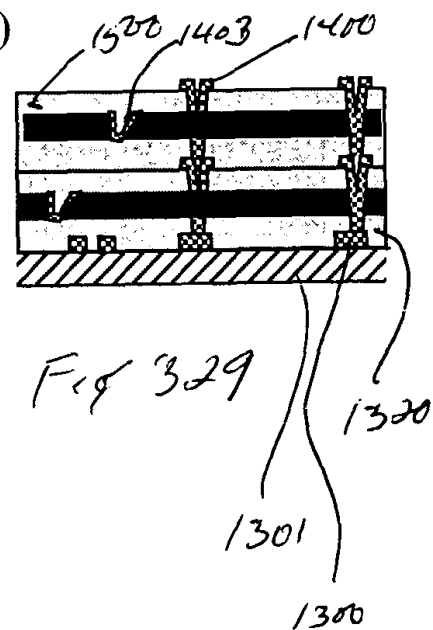
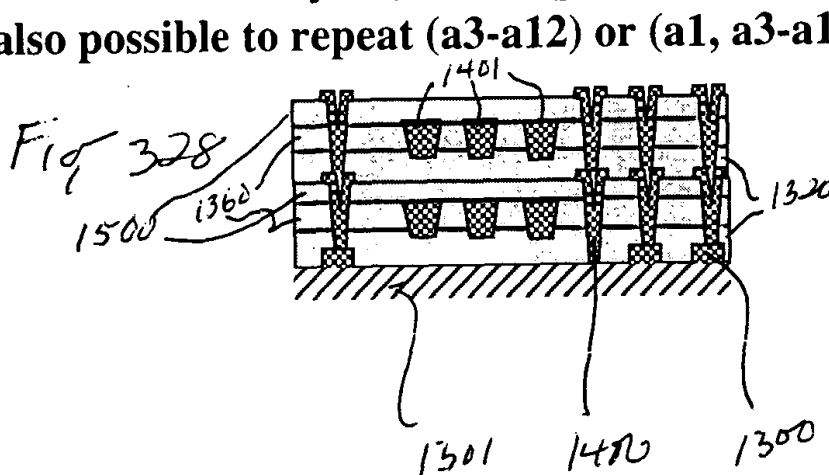
09767582.012201



1350c



In the case of multi layer (a1-a12) process is repeated on the (a12).
-it is also possible to repeat (a3-a12) or (a1, a3-a12)



Invented Corner Turning Structure (A)

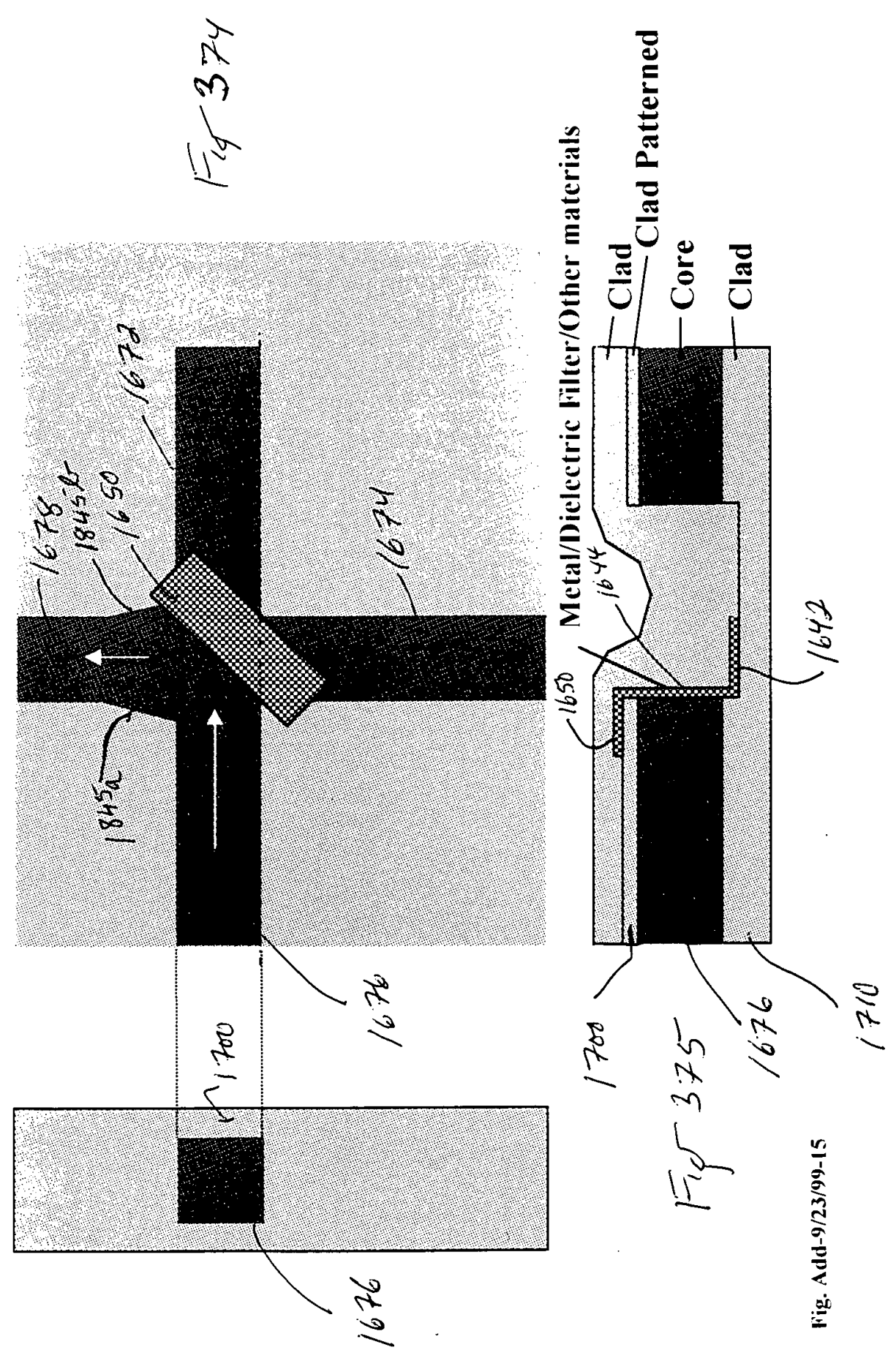
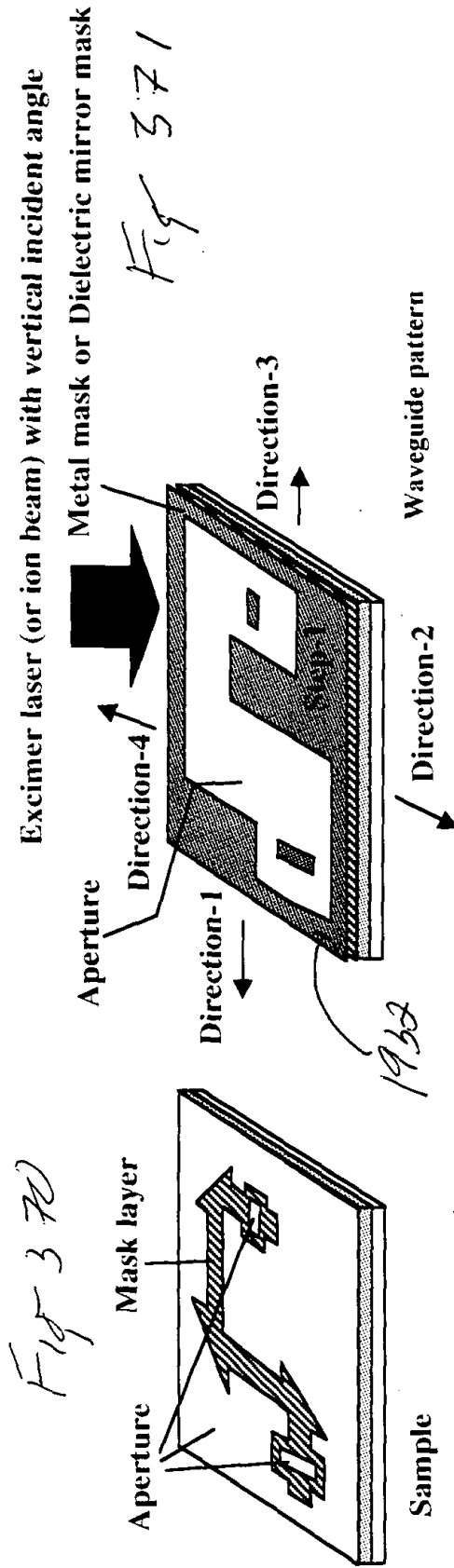
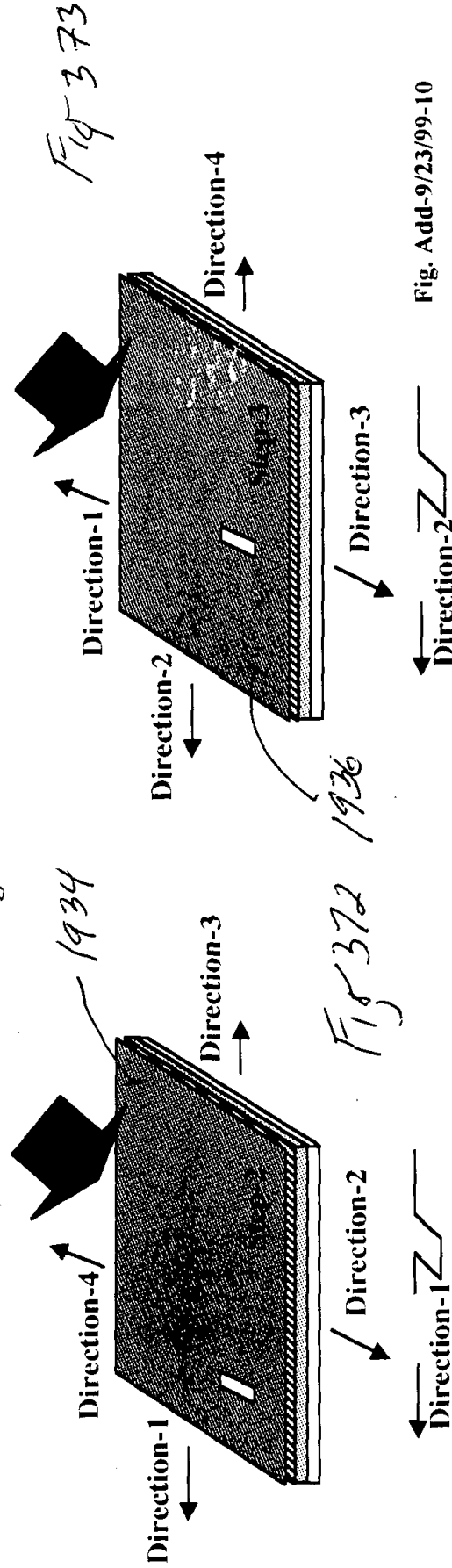


Fig. Add-9/23/99-15

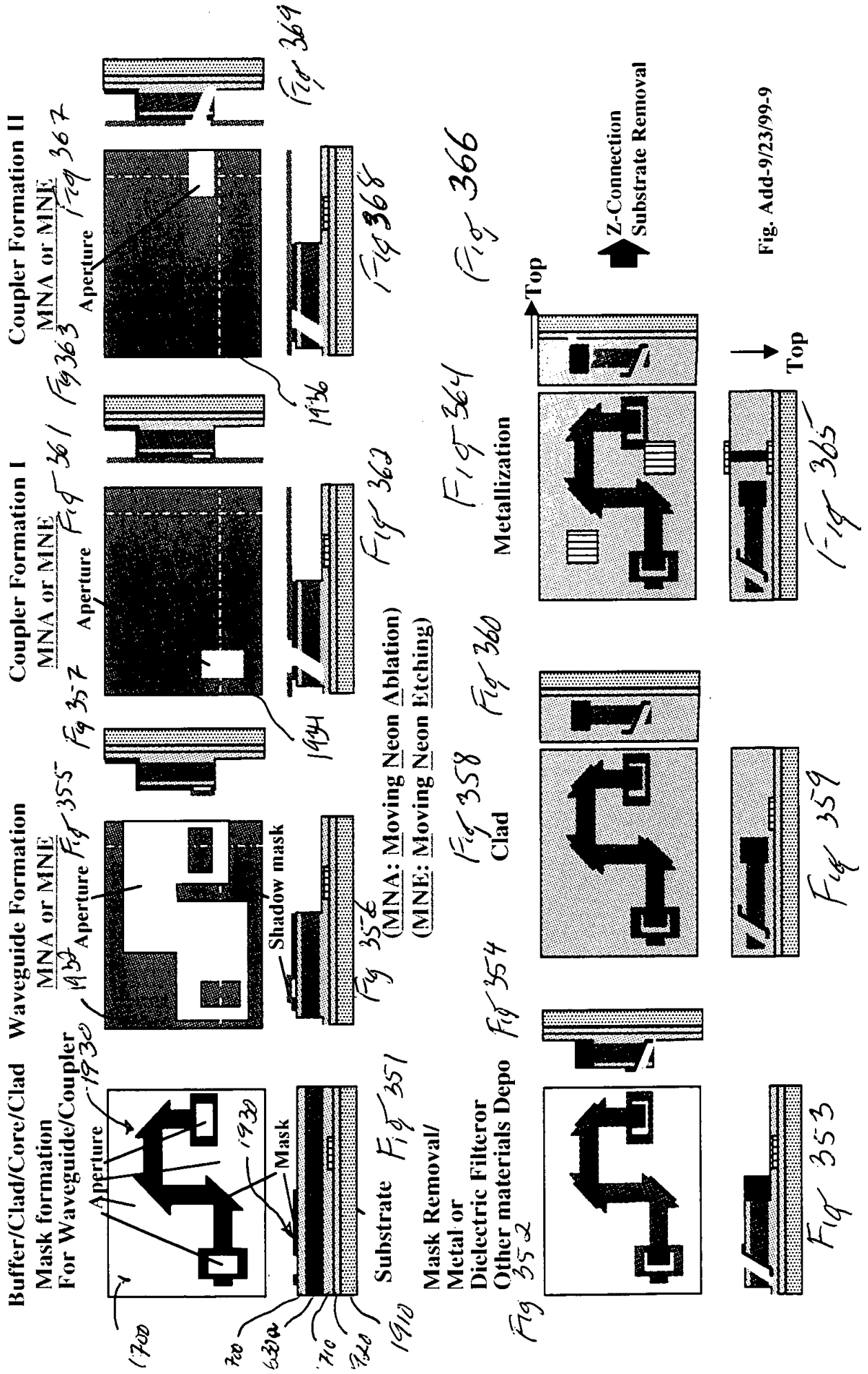
MNA, MNE Example for Add2 example



Excimer laser (or ion beam) with tilted incident angle



Another Process Flow for Structure (II)



Excimer Laser Ablation Example for Beveled Cut (2)

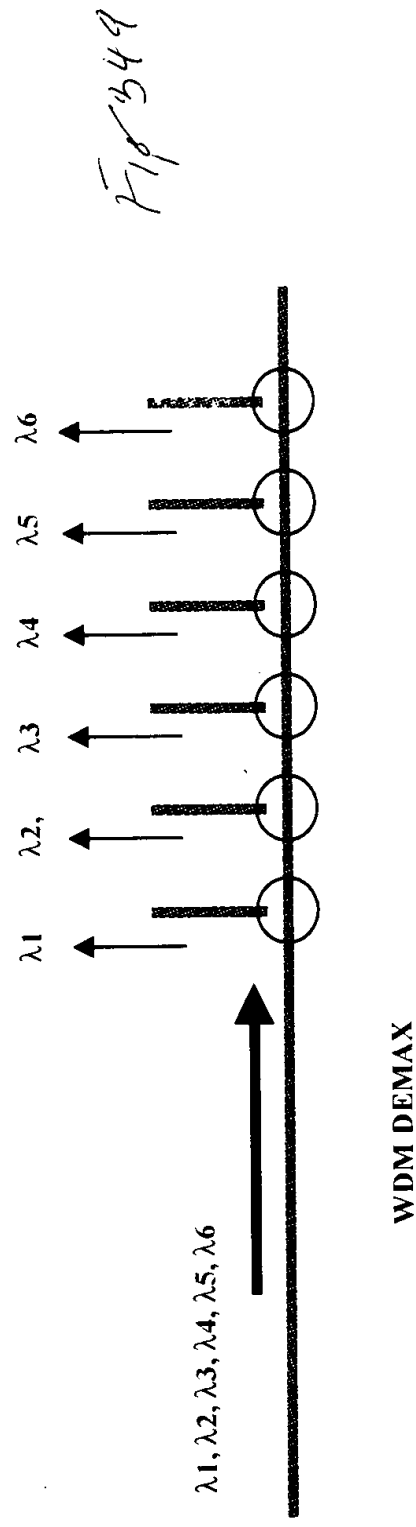
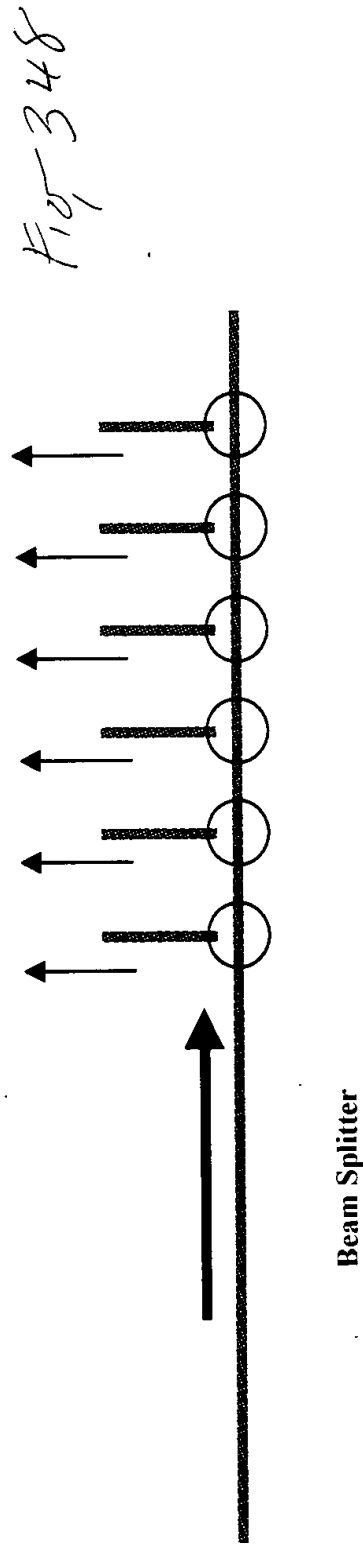


Fig. Add-9/23/99-8

Invented Coupler Structure (II)

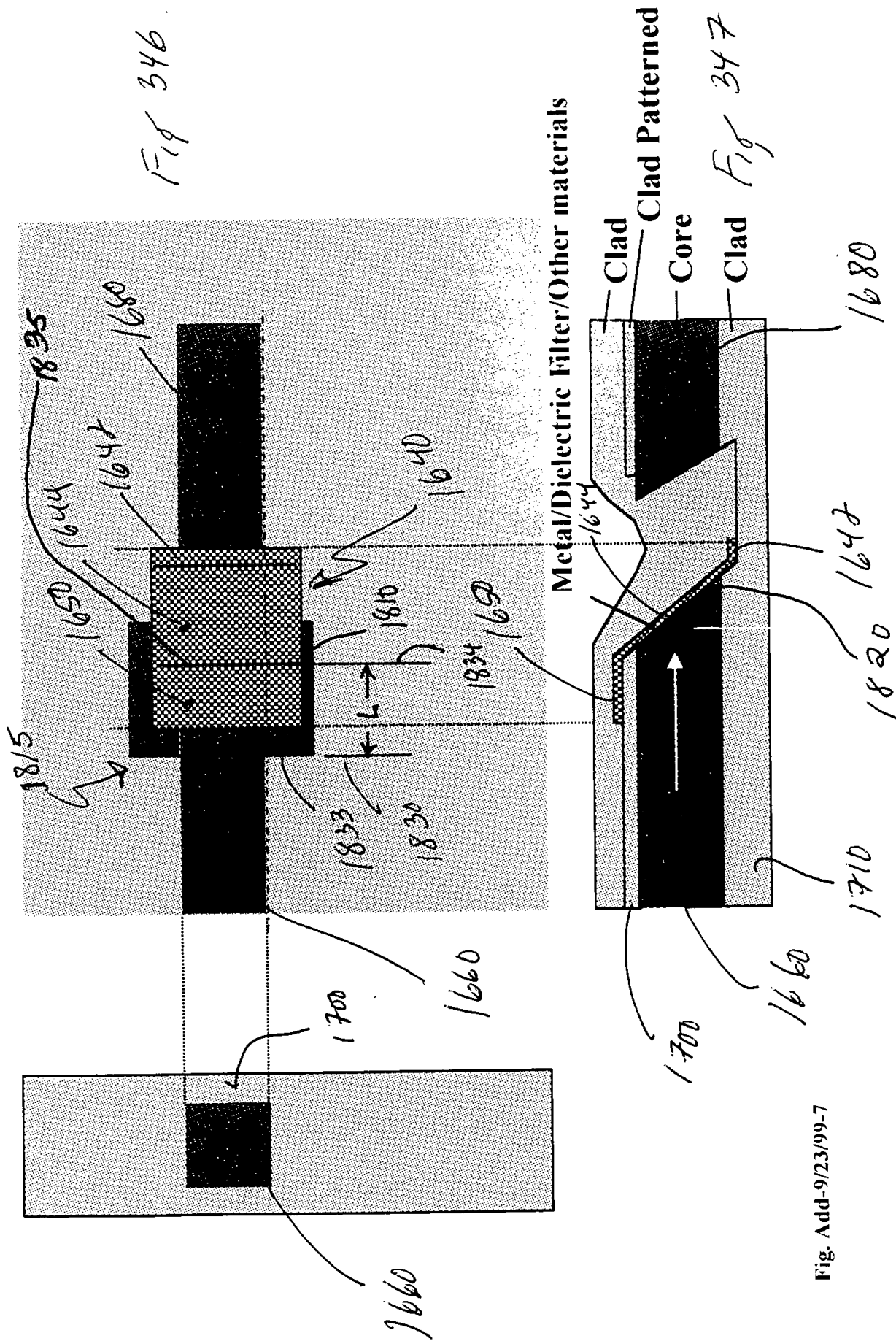


Fig. Add-9/23/99-7

Invented Coupler Structure (I)

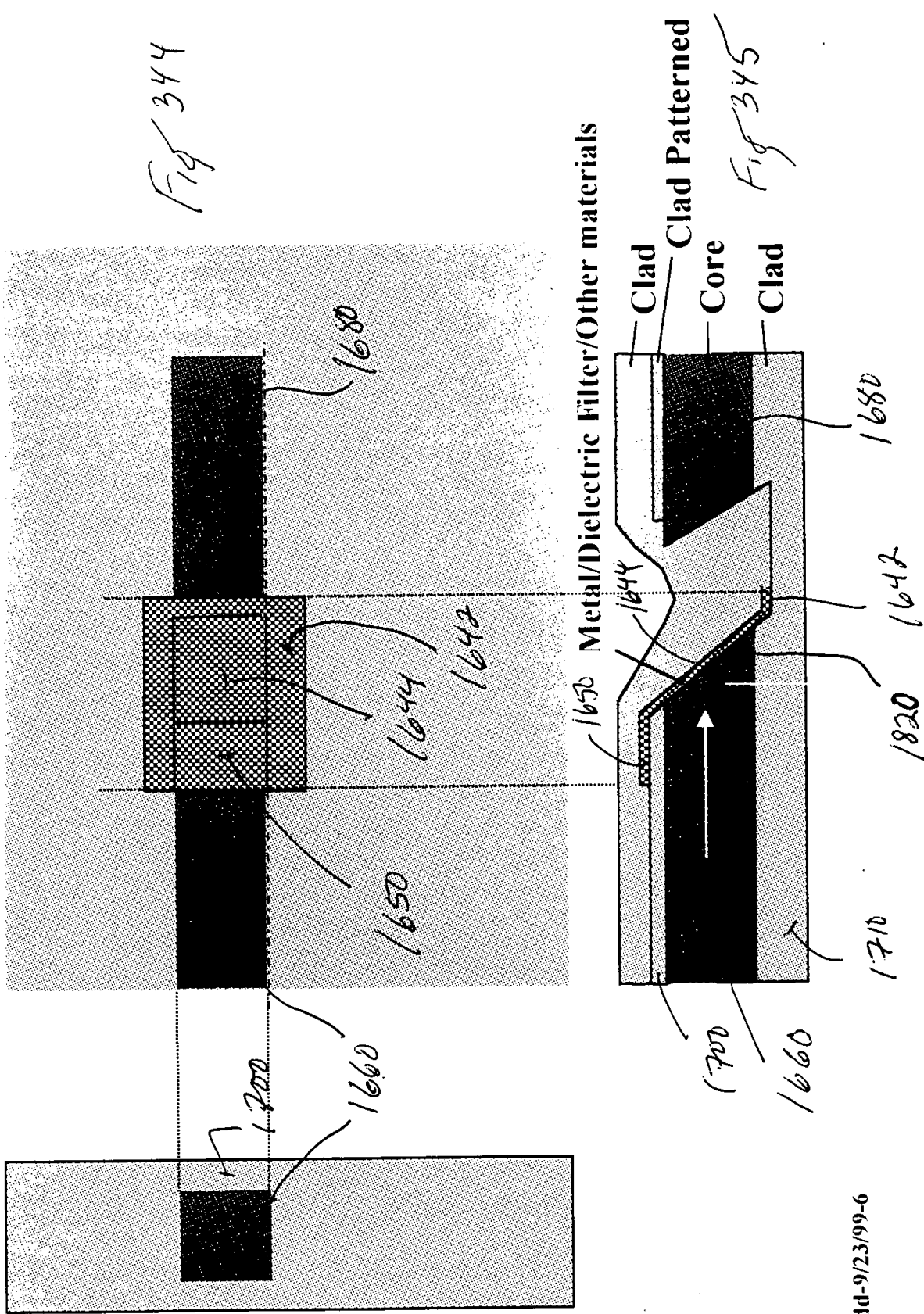


Fig. Add-9/23/99-6

Conventional Coupler Structure (I)

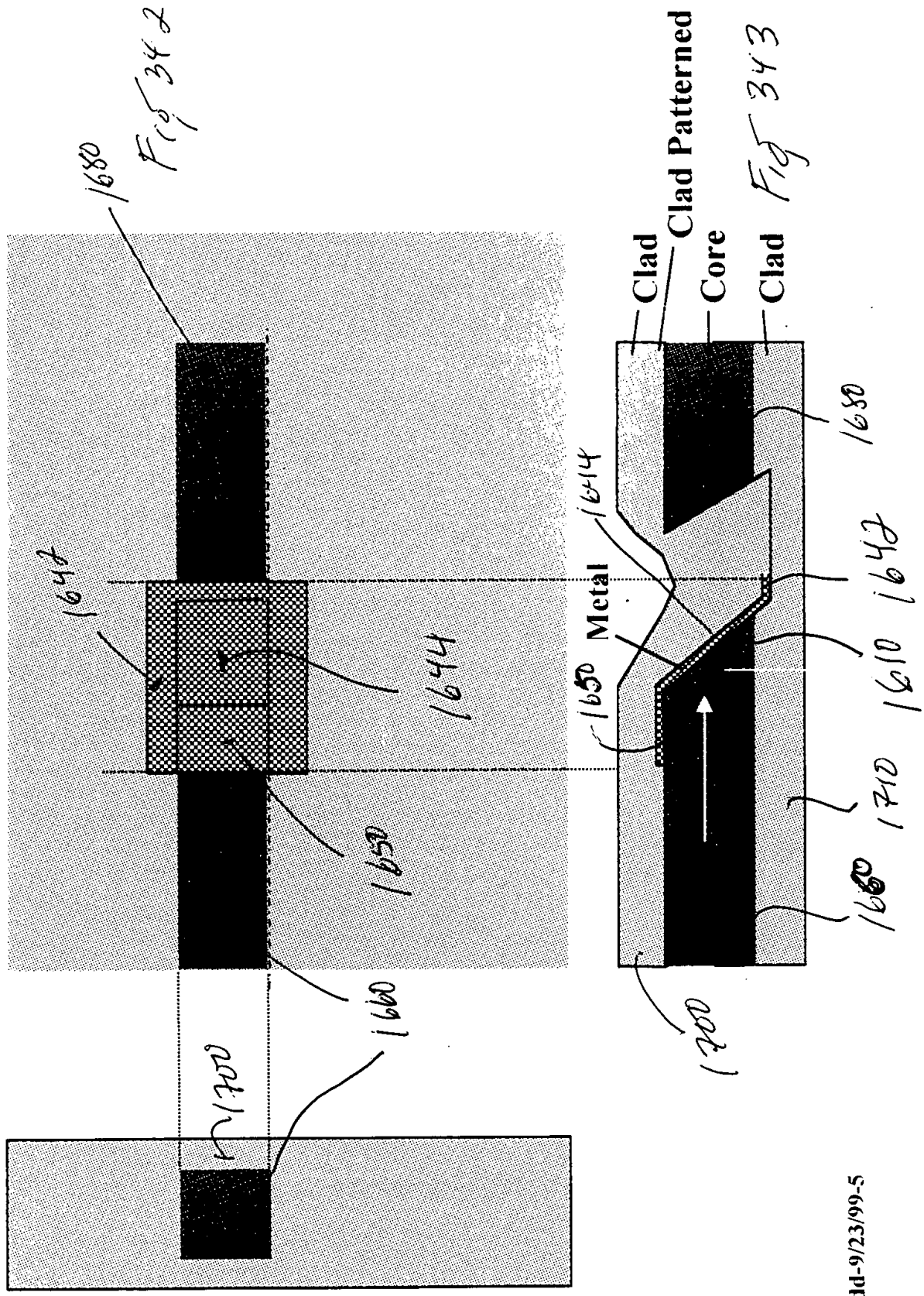


Fig. Add-9/23/99-5

Invented Corner Turning Structure (II)

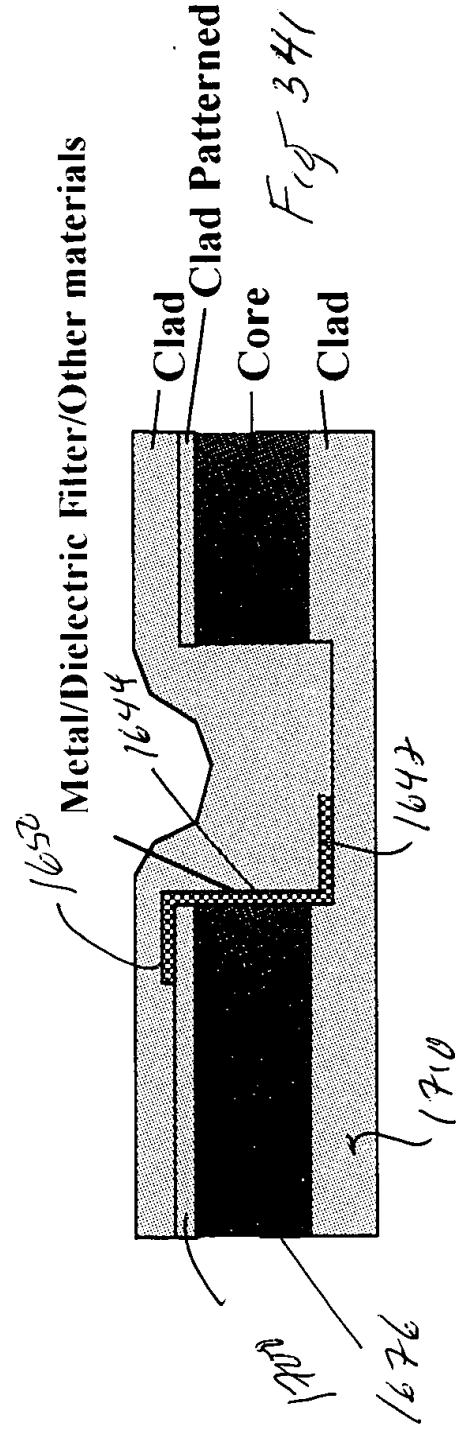
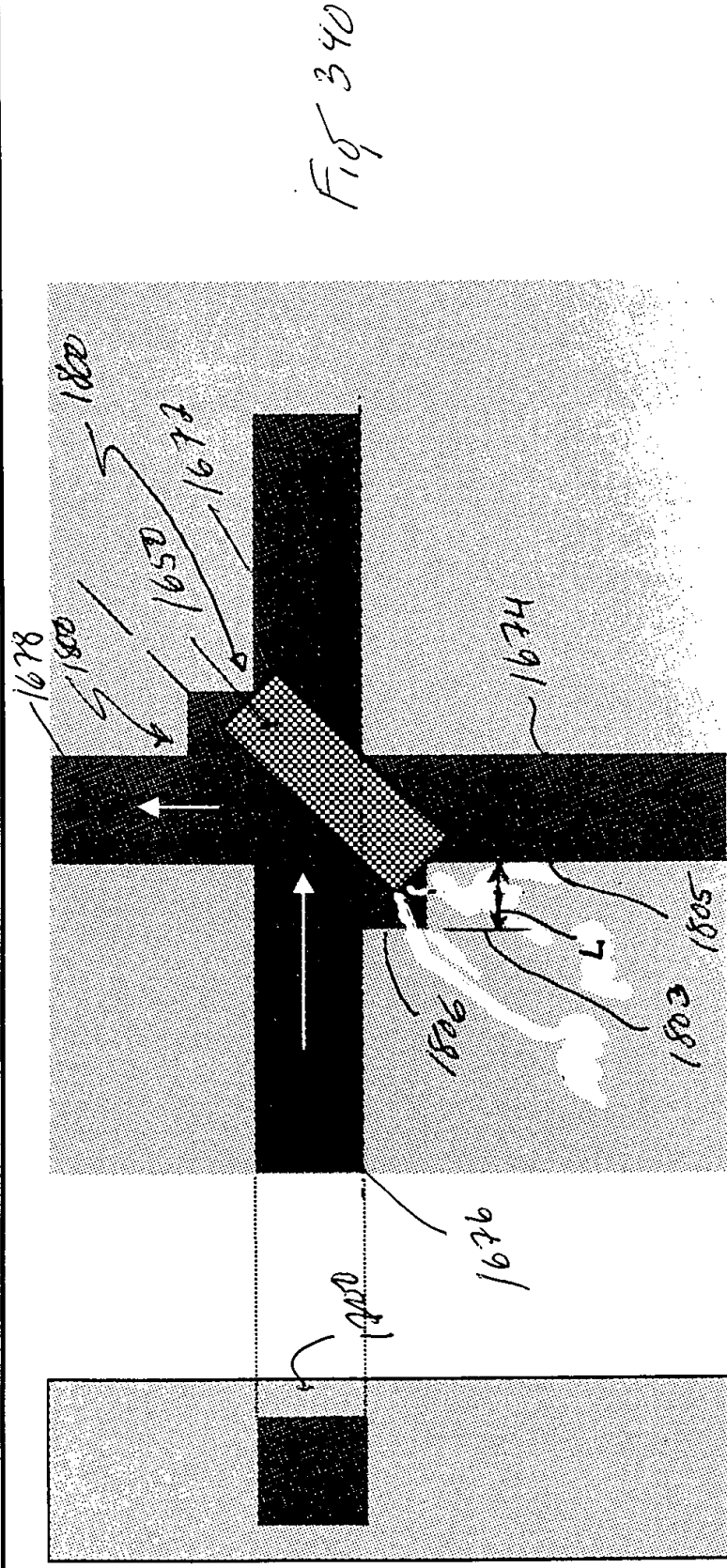


Fig. Add-9/23/99-4

Conventional Corner Turning Structure

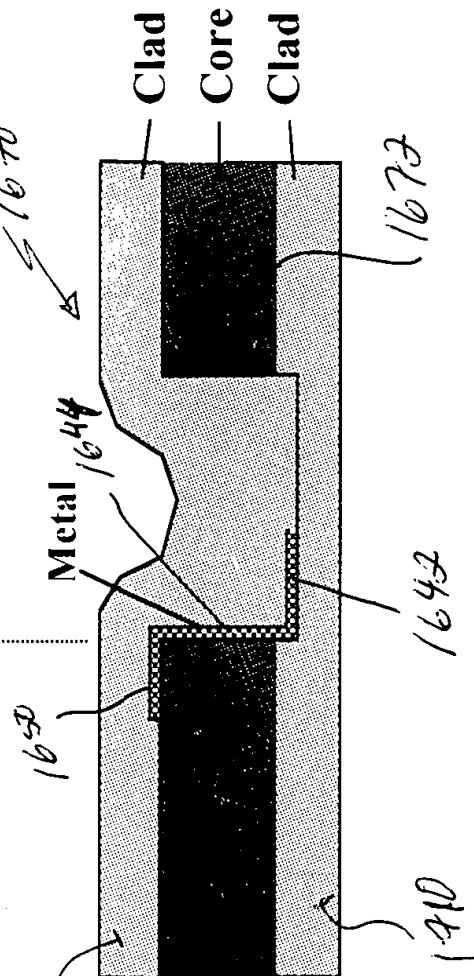
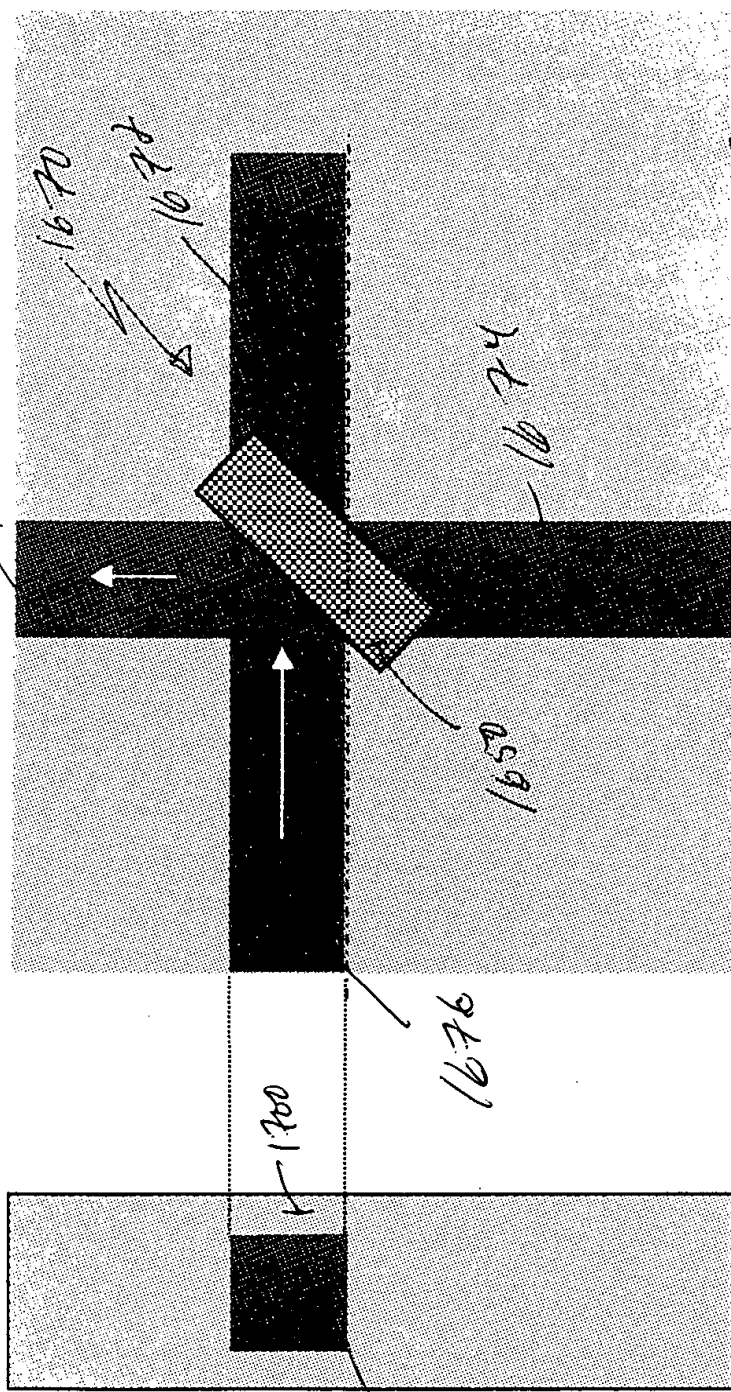
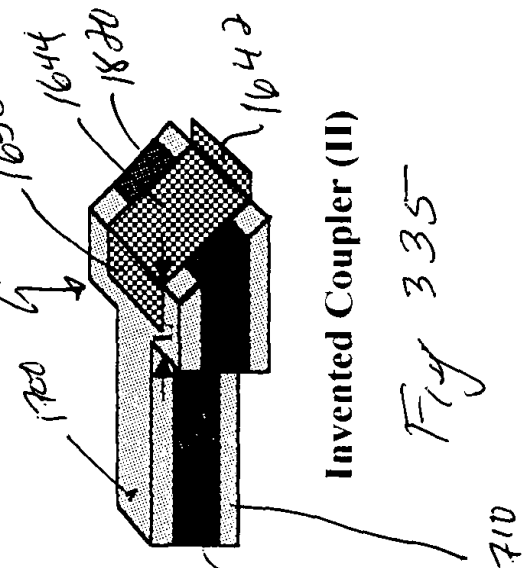
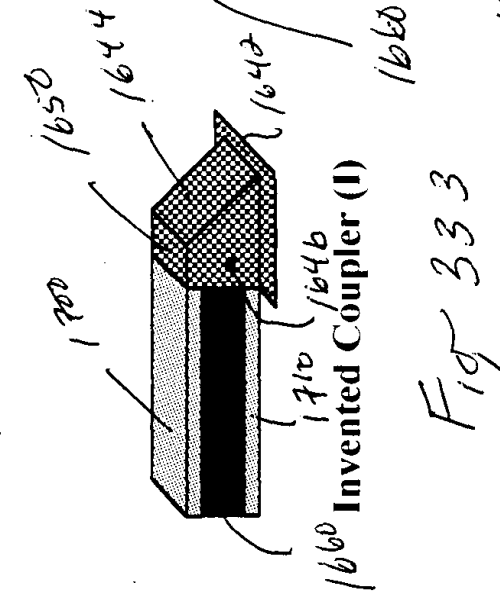
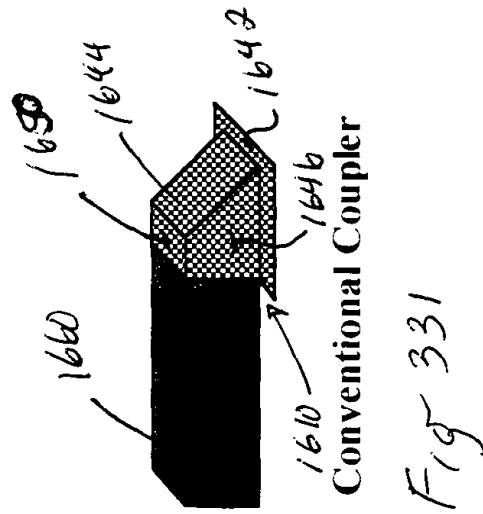
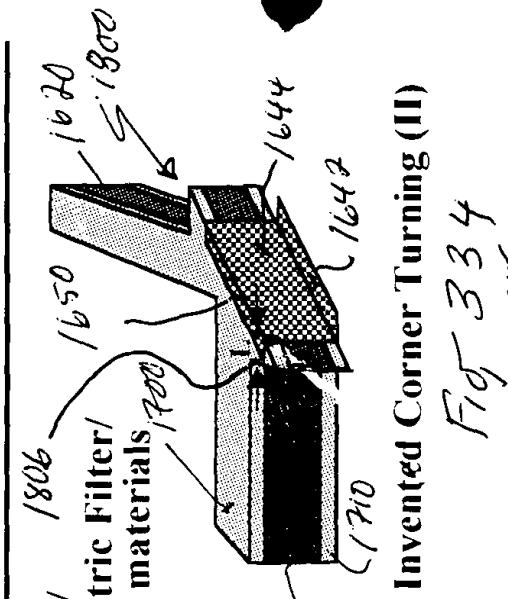
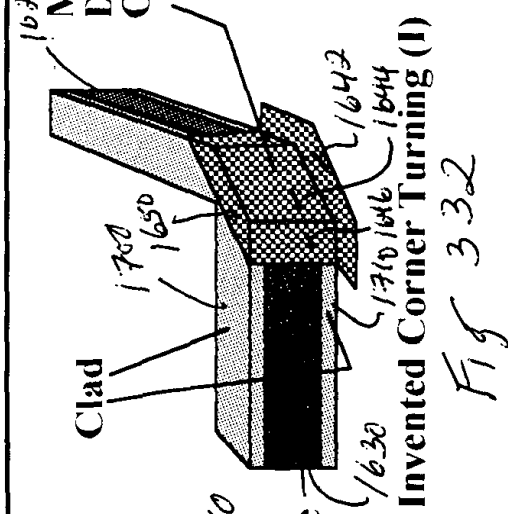
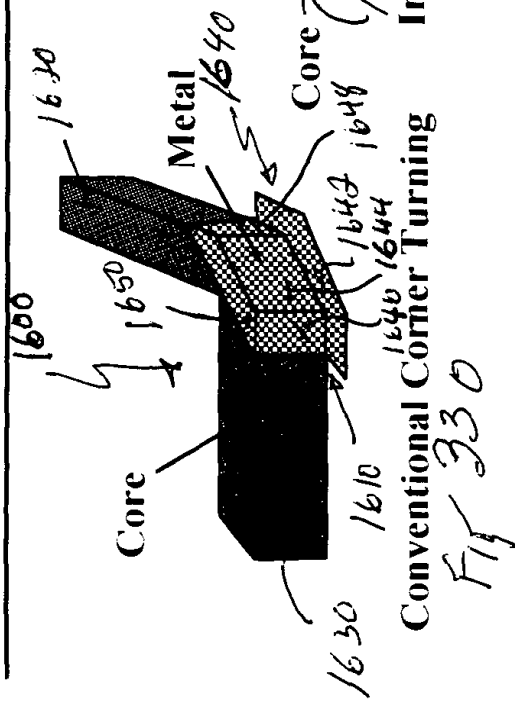


Fig. Add-9/23/99-2

Conventional and Invented Waveguide Structure Examples



Example 3: Z waveguide Fab. Process 1

(a1) Metal pattern formation

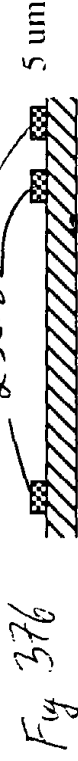


Fig 376

(a2) Core coat



Fig 378

(a3) Z-WG core patterning



Fig 380

[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

Development

(for AlliedSig, ORMOCERs)



Fig 382

(a4) Clad coat

(for planarization viscosity adjust if necessary CMP)



Fig 384

(a5) Core coat



Fig 386

[DuPont, AlliedSig, ORMOCERs or F-PI]

(a6) WG core patterning

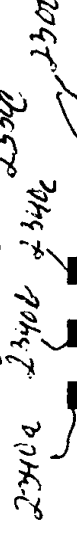


Fig 388

[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

Development

(for AlliedSig, ORMOCERs)



Fig 390

Fig 377



Fig 378



Fig 381



Fig 383



Fig 385



Fig 387



Fig 389

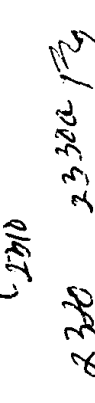


Fig 391

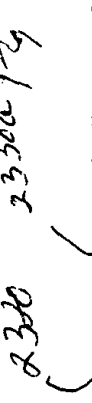


Fig 393



Fig 395

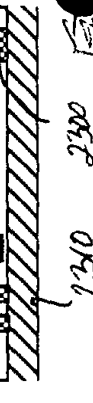


Fig 397

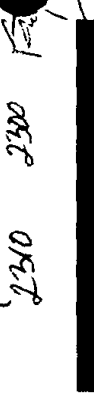


Fig 399



Fig 401

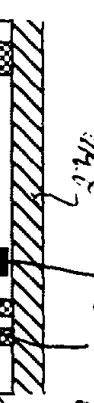


Fig 403

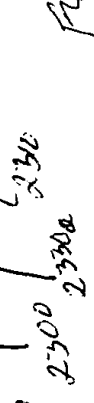


Fig 405



Fig 407



Fig 409



Fig 411



Fig 413

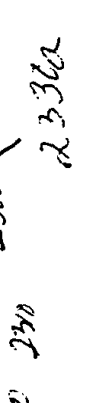


Fig 415

Example 4: Z waveguide Fab. Process

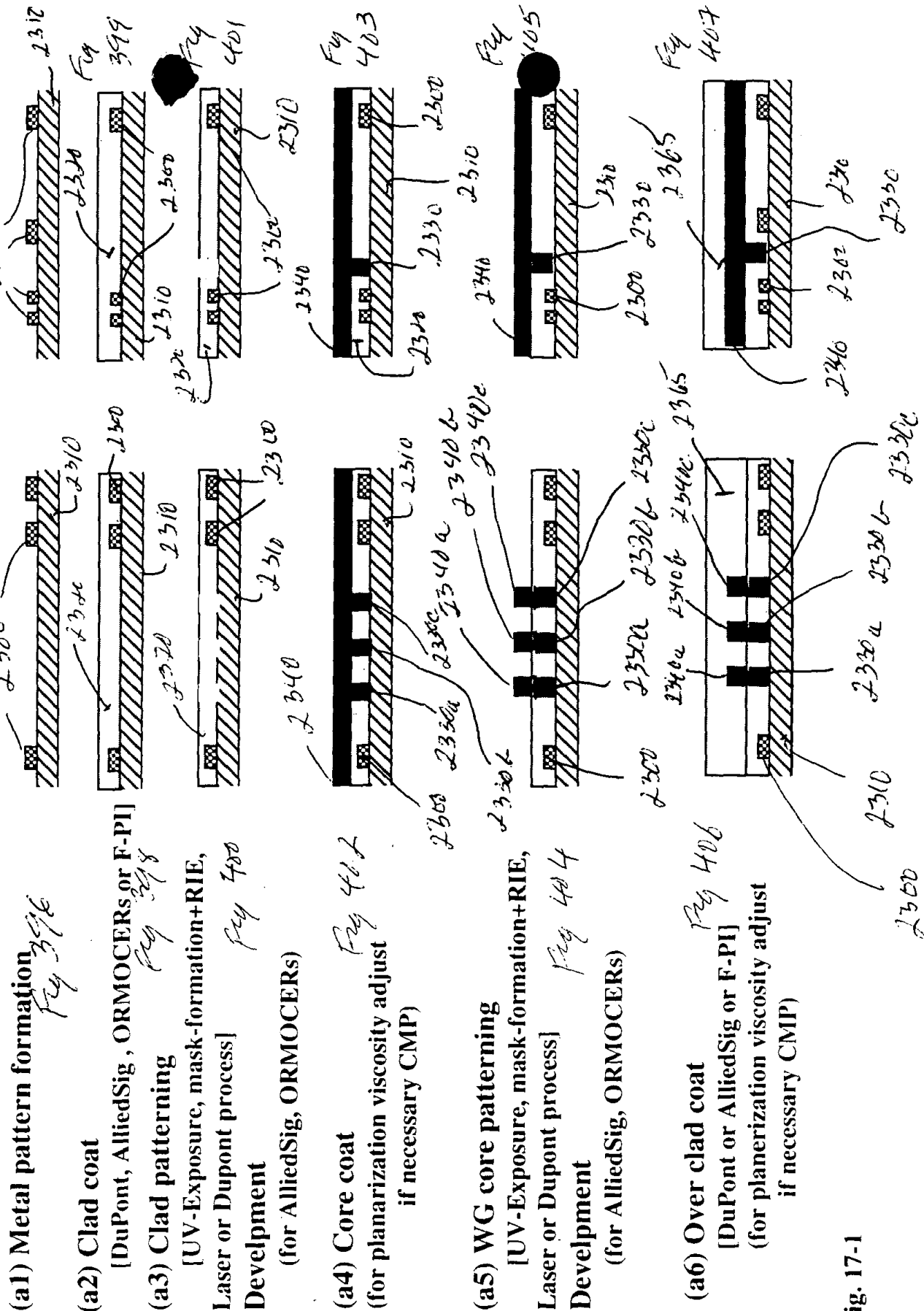
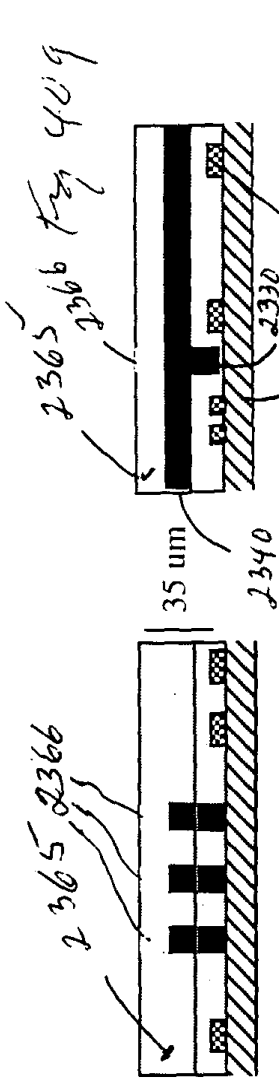


Fig. 17-1

(a7) Clad patterning

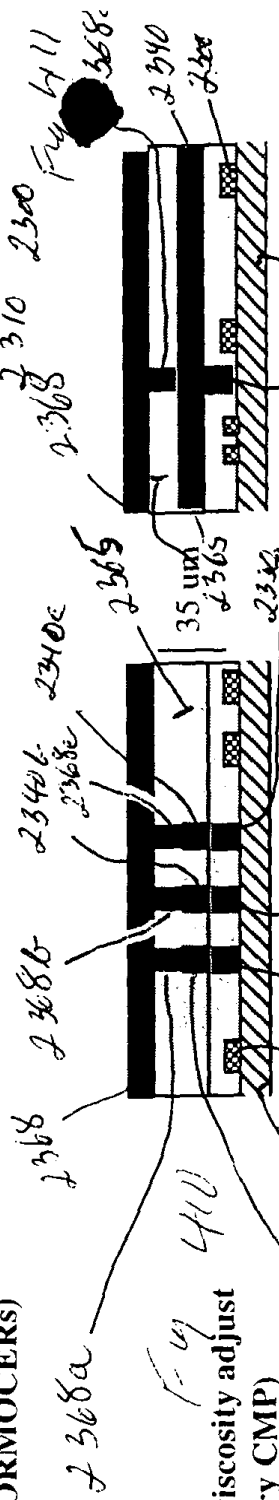
[UV-Exposure, mask-formation+RIE,
Laser or Dupont process] Fig 408
Development

(for AlliedSig, ORMOCERs)



(a8) Core coat

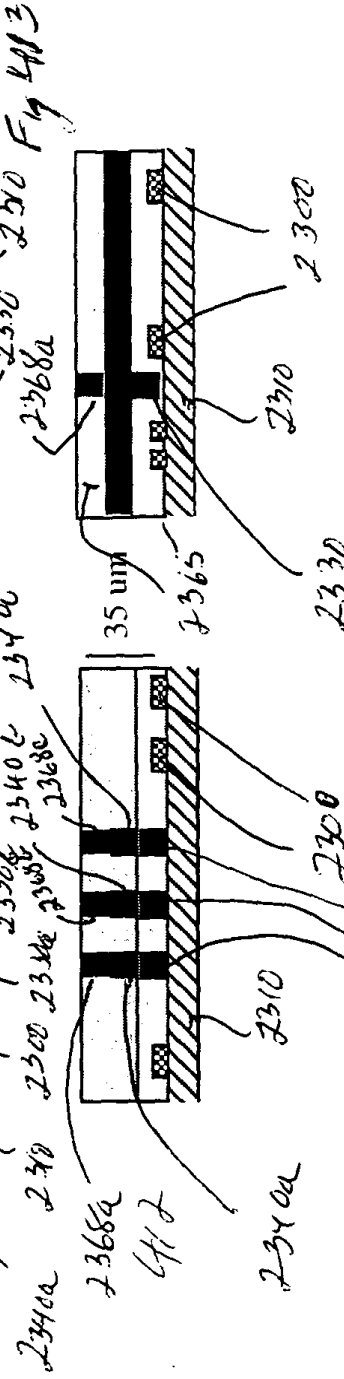
(for planarization viscosity adjust
if necessary CMP)



or

(a8) Core coat and CMP

Fig.



In the case of multi layer (a1, a5-a8) or (a5-a8) process is repeated on the (a8).

Fig. 17-2

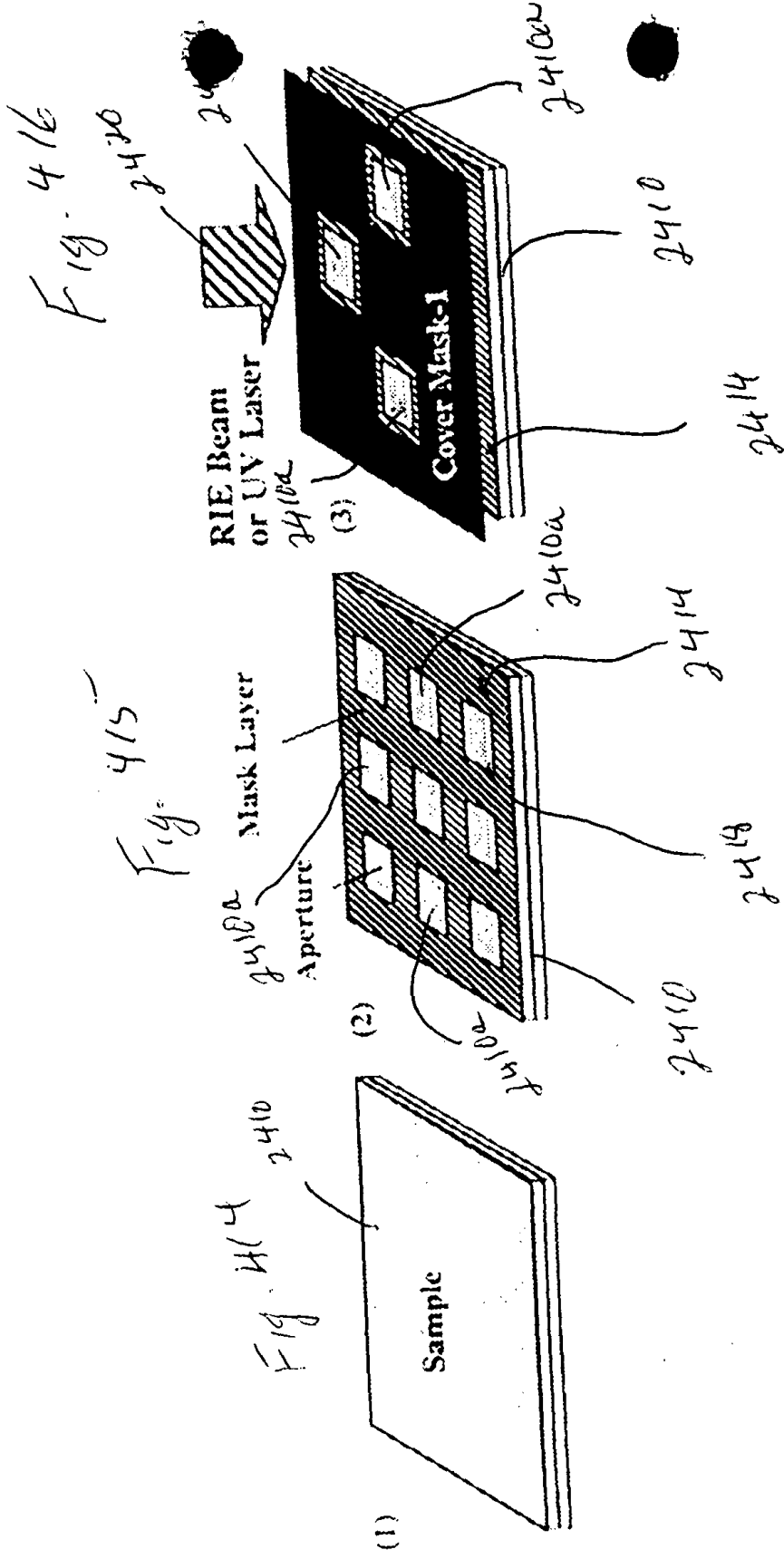


Fig. 4/5

Fig. 4/6

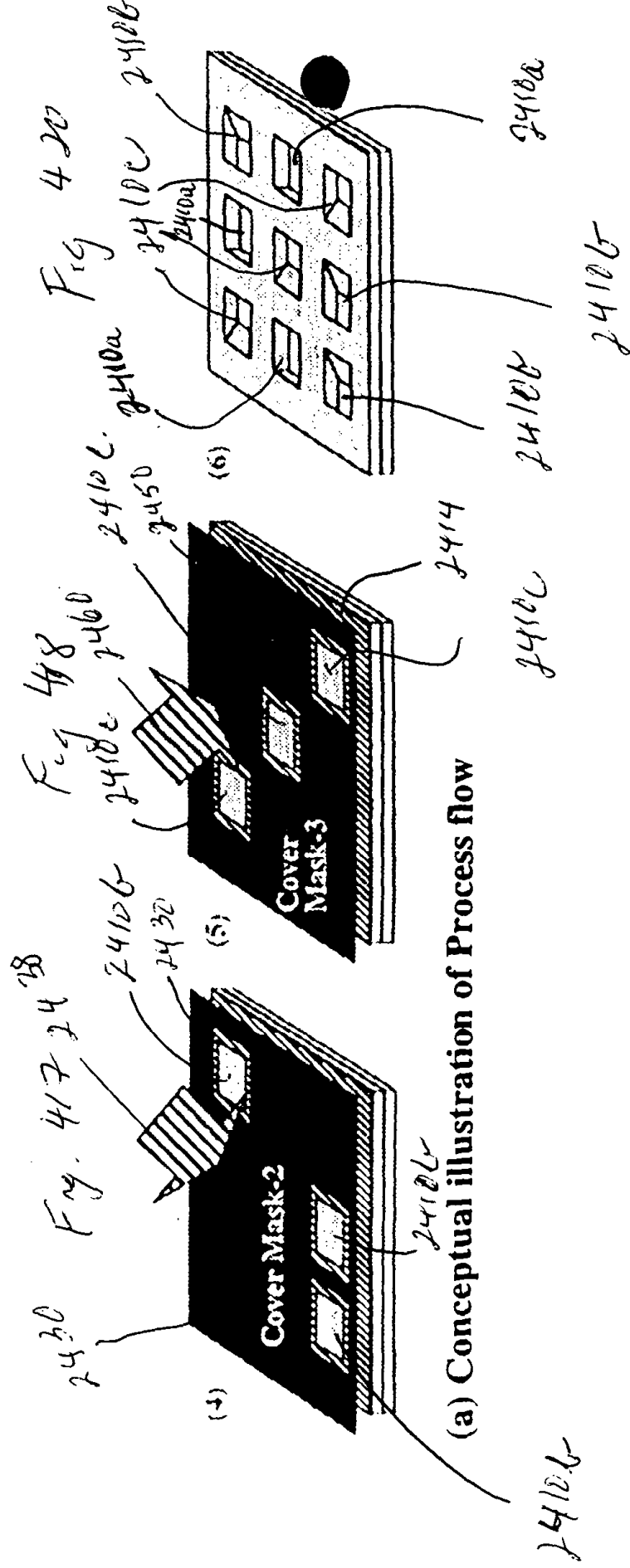
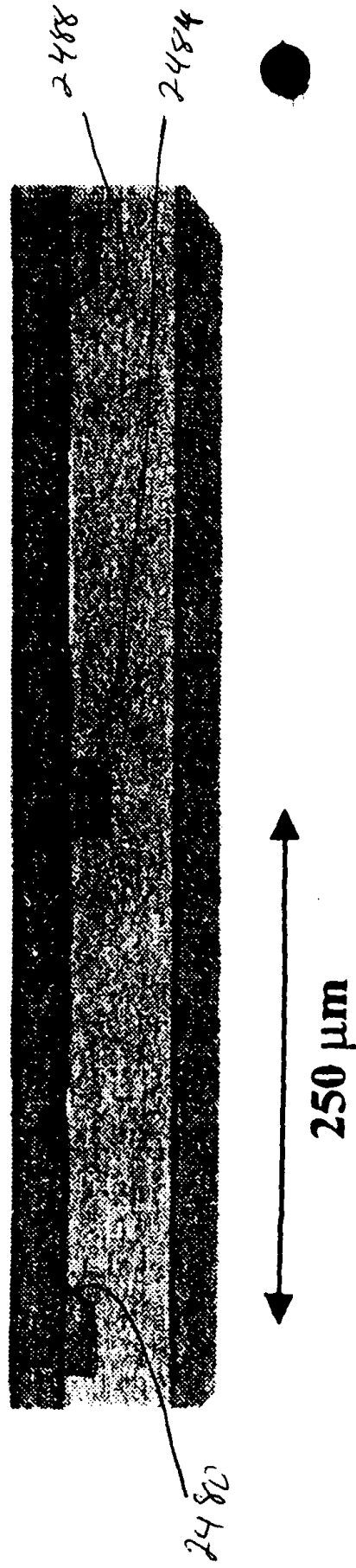


Fig. 4d1



(b) Trench wall formation of three different angles